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F. H. Eisen and S. I. Long
Principal Investigators

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This report covers a program on the development of a planar GaAs digital integrated circuit (IC) technology. The main goals of this program were the development and implementation of the fabrication technology, and the demonstration of the feasibility of reaching large-scale integration (LSI) with high-speed, low-power GaAs digital ICs. In approximately 3 1/2 years a planar fabrication process was developed and refined. The program started with the fabrication of the first planar FET transistors using the new process, and the demonstration of Schottky diode-FET logic (SDFL) gates, showing high speed operation of ring

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oscillators. After this initial stage, many logic circuits have been built. The complexity of these demonstration circuits, involving both combinatorial and sequential logic, grew at a nearly exponential rate. Among the most complex circuits fully demonstrated is a 5 x 5 bit parallel multiplier employing 260 SDFL gates. The circuit multiply time is 4 ns, corresponding to a propagation delay of 190 ps per gate, with a power dissipation of 0.7 mW/gate (for a power-delay product of 133 fJ/gate). Finally, an 8 x 8 bit parallel multiplier having 1008 gates was designed, fabricated and tested. Although no fully working circuit was found on the first few wafers tested, several circuits with over 1000 working gates were identified. These results demonstrate the feasibility of LSI (1000 gates) GaAs digital IC's employing SDFL circuits using the Rockwell planar fabrication process.

Although principally focused on the development of the process and the design, fabrication and test of demonstration circuits, this research effort also involved work in a number of material related areas. The bulk of this research effort was carried out at the Electronics Research Center (ERC) of Rockwell International with contributions from three subcontractors: Crystal Specialties, Inc. in GaAs substrate growth, the California Institute of Technology in ion implantation; and Cornell University in device modeling.

The report starts by addressing substrate material and ion implantation. This is followed by an overview of the fabrication process, a discussion of each one of the critical process steps, and an analysis of fabrication yield. Process monitoring techniques are also discussed. Circuit design is addressed starting from a discussion of the basic building block, the SDFL gate and circuit modeling techniques. This is followed by a discussion of design and measurement results for each type of circuit built, both of the sequential and combinatorial type. Preliminary efforts in circuit packaging and promising preliminary results from radiation and environmental testing are also reported.

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FOREWORD

The research covered in this report is carried out in a team effort having the Rockwell International Electronics Research Center as the prime contractor with two universities and a crystal manufacturer as subcontractors. The effort is sponsored by the Materials Science Office of the Defense Advanced Research Projects Agency. The contract was monitored by the Air Force Office of Scientific Research. The Rockwell program manager was Fred A. Blum. The principal investigators for each organization were:

Electronics Research Center	F.H. Eisen, S.I. Long
California Institute of Technology	J.A. Mayer, M.A. Nicolet
Cornell University	L.F. Eastman
Crystal Specialties	W.P. Allred

Numerous other researchers were involved in the work reported on. The principal contributors were:

Electronics Research Center	P.M. Asbeck, R.C. Eden, R.D. Fairman, A. Firstenberg, W.P. Fleming, J.A. Higgins, G.R. Kaelin, C.G. Kirkpatrick, C.P. Lee, F.S. Lee, M.J. Sheets, E.K. Shen, Y.D. Shen, E.R. Walton, B.M. Welch R. Zucca
California Institute of Technology	B. Paine, M. Grimoldi
Cornell University	M. Shur
Crystal Specialties	J. Burns, H. Olsen

TECHNICAL SUMMARY

This report covers a program on the development of a planar GaAs digital integrated circuit (IC) technology. The main goals of this program were the development and implementation of the fabrication technology, and the demonstration of the feasibility of reaching large-scale integration (LSI) with high-speed, low-power GaAs digital ICs. The program was very successful. In approximately 3-1/2 years the planar fabrication process was developed and refined. The program started with the fabrication of the first planar FET transistors using the new process, the demonstration of Schottky diode-FET logic (SDFL) gates, and showed high speed operation of ring oscillators. After this initial stage, many logic circuits have been built. The complexity of these demonstration circuits, involving both combinatorial and sequential logic, grew at a nearly exponential rate. Among the most complex circuits fully demonstrated is a 5 × 5 bit parallel multiplier employing 260 SDFL gates. The circuit multiply time is 4 ns, corresponding to a propagation delay of 190 ps per gate, with a power dissipation of 0.7 mW/gate (for a power-delay product of 133 fJ/gate). The yield of working circuits was as high as 25%. Finally, an 8 × 8 bit parallel multiplier having 1004 gates was designed, fabricated and tested. Although no fully working circuit was found on the first few wafers tested, several circuits with over 1000 working gates were identified.* These results demonstrate, without ambiguity, the feasibility of LSI (1000 gates) GaAs digital IC's employing SDFL circuits using the Rockwell planar fabrication process.

Although principally focused on the development of the process and the design, fabrication and test of demonstration circuits, this research effort also involved work in a number of material related areas. The bulk of this research effort was carried out at the Electronics Research Center (ERC) of Rockwell International. Valuable contributions were made by three subcontractors:

*While this report was in press, full operation of the 1008 gate muiltiplier was demonstrated + 6 bit products were obtained in 5.2 ns, corresponding to τ_d = 150 ps.

Crystal Specialties, Inc., in GaAs substrate growth, the California Institute of Technology in ion implantation; and Cornell University in device modeling.

The semi-insulating material used in this program has been supplied primarily by Crystal Specialties, Inc. In addition to supplying material, they have carried out experiments to investigate possible improvements in growth technology. Material from other suppliers has also been evaluated using qualification procedures discussed in Sec. 2.1 of this report. At the end of the program, preliminary evaluation of semi-insulating GaAs grown by the liquid encapsulation Czochralski (LEC) technique at ERC was carried out with very promising results. Significant progress has been made in interpreting the qualification results in terms of Cr outdiffusion effects. All these subjects are discussed in Section 2.0 of this report.

Ion implantation, treated in Section 3.0, has received great attention during the program. While the process development work was carried out using Se implantations for the FET channels, S implantations for the diodes, and combined implantations of Se and S for ohmic contacts, Si implantations have been actively investigated. This research covers both the use of Si as substitute for Se and S in low-dose implants, and the use of heavy doses of Si implants for ohmic contact regions. Other topics investigated in ion implantation include recoil studies, orientation effects, and low temperature anneals.

The rapid increase in complexity of circuits fabricated in this program is a clear demonstration of the efficacy of the ion implanted planar process developed. Important features of this process include the use of a dielectric layer to protect the GaAs surface during all processing steps, and the use of dry etching techniques which make the process compatible with the present 1 μm minimum feature size and possible further geometry reductions. A second layer metalization process which uses plasma deposited silicon nitride as the dielectric separating first and second layer metalizations has been successfully developed. These subjects are discussed in detail in Section 4.0, along with a discussion of process yield.

Great efforts have been made to monitor the results of the fabrication process in an effective feedback mode. This was done by dedicating 16% of the area of each wafer to a number of test structures designed to monitor each process step, and to evaluate uniformity and reproducibility of device parameters. Automatic test equipment was used to gather and analyze a large volume of data. This process monitoring approach and resulting statistical data are discussed in Section 5.0

Five mask sets have been designed in this program. The first mask set contained many test structures and simple test circuits for process evaluation, and ring oscillators. The following masks still contained test structures and ring oscillators, but they also had demonstration circuits of increasing complexity. The second mask set was highlighted by an 8:1 data multiplexer and the corresponding 1:8 demultiplexer, and a frequency dividers (÷8). The third mask set contained improved versions of the circuits on the previous mask plus an 8-stage shift register and a 3 × 3 bit parallel multiplier. The gate counts on mask sets 2 and 3 reached ~ 100 gates. The fourth mask set contained a 5 × 5 bit parallel multiplier (260 gates) and a 64-stage shift register (540 gates). The fifth and last mask set contained the 8 × 8 bit parallel multiplier with 1008 gates. Section 6 contains a description of those demonstration circuits and a discussion of their evaluation. Work in circuit packaging and very encouraging preliminary results from radiation hardness tests are also discussed in this section.

The principal conclusion emerging from the data presented in Section 6 is that the feasibility of producing circuits with up to 1000 gates operating at propagation delays of ~ 150 ps/ gate, with average power dissipation below 1 mW/gate using a planar GaAs technology has been demonstrated. The performance figures quoted are quite conservative, and they have been comfortably met by the MSI/LSI demonstration circuits. Projections for the future can be made based on the results from small circuits and ring oscillators. These data show that SDFL circuits are capable of propagation delays of 62 ps (demonstrated for a power-delay product of 65 fJ) and that power dissipation can be as low as 16 fJ/gate (for a propagation delay of 136 ps). Further gains in terms of overall circuit

operating speed and power dissipation can be achieved with circuit design improvements made possible by multi-level logic. The capability of the process developed under this program for implementing multi-level logic circuits has already been demonstrated.

1.0 INTRODUCTION

The performance advantages offered by GaAs integrated circuits in the areas of speed, power dissipation and radiation hardness place it as a prime candidate for the device technology of next generation military electronic systems. Advantages in both speed and power are derived from the superior material characteristics of GaAs when compared to silicon. The electron mobility in GaAs is approximately 5 times that in correspondingly doped silicon, and almost 10 times the mobility of silicon grown on sapphire. The fabrication of GaAs integrated circuits on a semi-insulating substrate results in a reduction of stray capacitances leading to a significant improvement in power dissipation. These two factors; the high electron mobility of GaAs and the availability of semi-insulating substrate material form the basis from which GaAs integrated circuits, operating at significantly higher speeds and with much lower dynamic switching energy, can be derived.

Although the fundamental advantages of GaAs over Si have been recognized for a long time, lack of processing techniques capable of the uniformity and reproducibility required for large scale integrated circuits (ICs) prevented the applications of GaAs devices from reaching beyond discrete microwave transistors and diodes. This situation changed in 1977 with the dramatic progress made in ion implantation in GaAs, coupled with better control of the substrate material.[1] Once ion implantation became a reliable processing technology it became feasible to conceive a planar fabrication technology capable of the high yield required for a new generation of high-speed low-power digital integrated circuits. It was also recognized, at that time, that in order to make a significant impact on the electronic systems of the 80's, the new technology should be capable of large scale integration (LSI) almost from the outset, rather than gradually increasing circuit complexity over a period of many years.

The program here reported was launched under the above premises. This ambitious three year program represents a large investment of financial and human resources. Starting from a solid base of substrate material and ion implantation control, a sound idea on a planar fabrication process, a new circuit approach (SDFL for Schottky-diode-FET logic), the goal was to develop

the technology and demonstrate the feasibility of a new generation of digital integrated circuits with LSI complexity (1000 gates). This goal has been met. Figure 1.0-1 is a photograph of an 8 × 8 bit parallel multiplier having 1008 gates, operating at a propagation delay of τ_D = 150 ps for a multiply time of 5.2 ns. Typical power dissipation for this technology is well below 1 mW/gate. Along with this outstanding result, a variety of MSI/LSI demonstration circuits with exciting potential applications have been built as circuit complexity was growing at an exponential rate during the program.

In order to meet the challenge of this ambitious program a task force capable of simultaneously attacking all aspects of the project was assembled. This included a sustained effort in material qualification and characterization, and in refinements of the ion implantation techniques. While the bulk of the effort was devoted to the development of the fabrication process, including 1 μm line lithographic techniques, metallization, and dielectric processes, a substantial investment was made in process monitoring techniques. At the same time, design rules and concepts had to be developed for the SDFL circuits, and modeling techniques had to be implemented. The success of the program must be credited to a great extent to the realization that all these contributing factors had to be attacked at once in order to achieve rapid success. Three subcontractors were integrated into the team. These were Crystal Specialties, Inc., providing material support, and the California Institute of Technology and Cornell University providing expertise in the areas of ion implantation and device modeling, respectively.

A leading concept in this program was the idea that a fabrication process could be developed and refined only by actually processing large numbers of wafers. Therefore, a small fabrication line, with capability for a steady flow of wafer fabrication was implemented. Approximately 150 wafers, plus many other experimental runs, were processed in this facility for this program. This volume made it possible to maintain a steady rate of wafer production, and gradually incorporate process refinements, allowing enough time for judging results from statistical rather than individual observations of the effects.

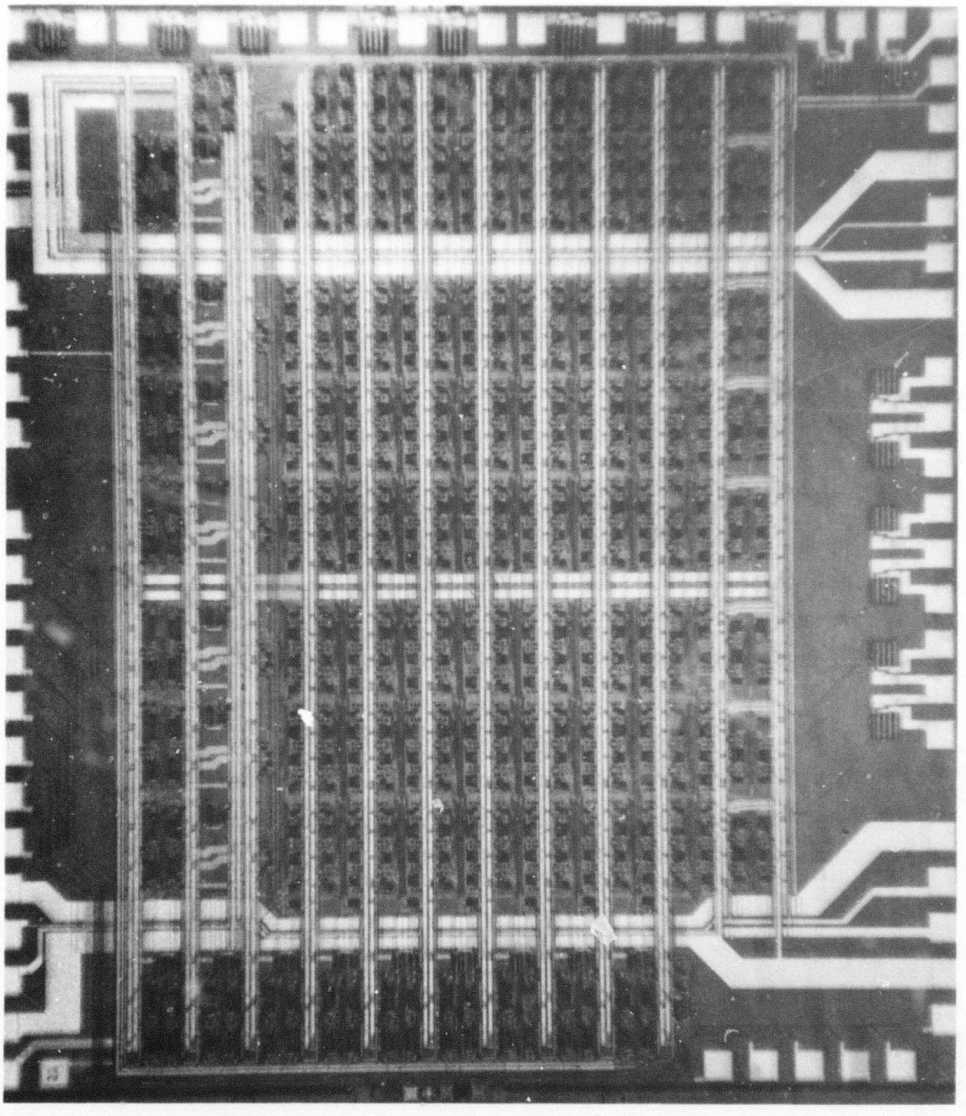


Fig. 1.0-1 Photograph of the CD chip on mask set AR4, showing two 5 × 5 bit multipliers and a 64-stage shift register.

The rapidly growing complexity of the circuits required a steady activity in circuit design and modeling. Five masks were designed and used during the program. The content of the masks has evolved significantly. While the first mask set was rich in experiments on circuit and device design, variety has been gradually replace by complexity as the circuits grew in size, and design rules became more and more firm. While in mask set AR1 a 2.25 × 2.25 mm chip contained approximately 25 different small circuits or design test structures, in the last mask set, AR5, a larger (2.7 × 2.7 mm) chip was almost fully occupied by one LSI circuit (the 8 × 8 multiplier).

The organization of this report follows the logical steps in the conception of an integrated circuit. The report starts with the substrate material, in Section 2.0, and the ion implantation technology in Section 3.0, Section 4.0 contains an overview of the fabrication process followed by a discussion of each one of the critical process steps, and an analysis of fabrication yield. Process monitoring techniques are discussed in Section 5.0. Section 6.0 covers circuit design starting from a discussion of the basic building block, the SDFL gate and circuit modeling techniques. This is followed by a discussion of design and measurement results for each type of circuit built, both of the sequential and combinatorial type. Preliminary efforts in circuit packaging and promising preliminary results from radiation and environmental testing are also reported in Section 6.0. Finally, Section 7.0 contains a list of the numerous publications which emerged from this program.

2.0 SEMI-INSULATING MATERIAL

GaAs material supply is an issue of critical importance. In order to aid in the selection of material, proven qualification tests have been developed and utilized. The progress of various suppliers of ingots grown by the horizontal Bridgman method have been monitored and material evaluated. Working with Crystal Specialties, techniques and analysis have been applied to improving Bridgman growth. The purchase and operation of a new Metal Research crystal puller for liquid encapsulated Czochralski (LEC) growth is expected to assist in improving the material supply. Preliminary results from LEC materials grown in the new system have been encouraging. The potential of both LEC and Bridgman materials for extension to large wafers have been considered, with research on the growth of GaAs material oriented toward meeting IC requirements. Section 2.1 covers growth of semi-insulating GaAs by the Bridgman technique as well as qualification techniques and results. Section 2.2 contains preliminary evaluation data from LEC materials. Section 2.3 contains a discussion on substrate preparation for the planar IC fabrication process.

2.1 Bridgman Material

During this program, the principal source of semi-insulating substrates has been Cr doped GaAs ingots grown by the Bridgman technique. The majority of these ingots were supplied by Crystal Specialties, Inc., a subcontractor under this program. Ingots from a variety of other suppliers were also evaluated in order to monitor progress and developments in Bridgman growth.

As in earlier work,[1] variability was observed in the behavior of different ingots in the ion implantation process. As a result, ingot selection has continued to be important in order to maintain reproducibility in circuit fabrication. The qualification procedures were extended to encompass (a) an isolation test, which consists of encapsulation of samples with Si_3N_4 followed by annealing without implantation (an ingot is rejected if a surface conducting layer is formed); and (b) representative Se n^- implants (such as would be used for FET channels). In the latter test, the resultant electron density profiles are monitored with particular attention to the degree of tailing of the profile.

It was found in all but 13 of 109 wafers tested that there was a one-to-one correspondence between the formation of conductive layers ("surface conversion") and the presence of deep tails in the carrier profiles. This supports the hypothesis that both are the result of an additive excess donor density, characteristic of the ingot, introduced during the anneal. By studying the distribution of the excess donor density it was determined that its appearance is the result of residual donors in the material which become undercompensated near the surface due to Cr redistribution. This redistribution effect is described more fully in Section 3.1. For ingots to be qualified for the IC process, the density of residual donors, N_{Dr}, must be sufficiently low, typically below 6 - 7 x 10^{15} cm^{-3} for a bulk Cr concentration, N_{Cr}, of 2 x 10^{16} cm^{-3}. An approximate analysis based on the observed characteristics of Cr diffusion suggests that the upper limit on residual donor density, $N_{D_r max}$, follows the relation $N_{D_r max} \sim N_{Cr}^{2/3}$, for an 850°C 30 min anneal.

The percentage of ingots tested that passed qualification varied among the different suppliers. Table 2.1-1 summarizes the qualification yields obtained over the past 21 months. Crystal Specialties has had by far the highest yield (56%), which represents an increase over the average obtained in the previous phase of this program, despite the fact that the requirements were made more stringent.

Table 2.1-1

Fraction of Ingots Tested That Passed Qualification for the Ion Implantation Process (October 1978 through June 1980)

Supplier	Ingots Qualified	Ingots Tested	Yield
Crystal Specialties, Inc.	14	25	56%
Mitsubishi-Monsanto Chemical Co.	5	13	38%
Sumitomo Electric Industries, Ltd.	0	7	0%
Morgan Semiconductor	0	2	0%

The most important factor in obtaining qualified ingots appears to be the reduction of Si contamination in the melt due to the quartz growth boat and ampoule. Direct chemical measurements of Si at the levels of interest (10^{15} - 10^{16} cm^{-3}) has proven very difficult. However, bulk analysis by the SIMS technique (by Charles Evans & Associates) is a developing technique which appears to have the requisite sensitivity not only for Si but for most other impurities believed to be important in semi-insulating GaAs (with the exception of oxygen). Preliminary results (Table 2.1-2) indicate that the Si concentration tends to be lower towards the tail (last to freeze) section of Crystal Specialties ingots (for both Cr doped or undoped melts), contrary to expectations from published distribution coefficients. This phenomenon, currently not understood, is in agreement with the tendency for the tails of marginal ingots to pass the qualification tests while the fronts fail. Results suggest also that the sulphur content of the ingots may be high enough to be of significance in qualification ($2 - 5 \times 10^{15}$ cm^{-2}). A study of ingots grown with As (believed to be the primary source of S contamination) from 4 different suppliers, however, did not indicate any variations in the S content of the ingots.

An important consideration for uniformity and reproducibility in circuit characteristics is the uniformity of the semi-insulating ingots, both along ingot length and across a slice. It has been noted that samples from the front (seed end) portion of ingots typically show lower qualification yield than corresponding tail samples. For use in the IC process, only ingots that pass the tests at both ends are accepted. Studies were carried out on the uniformity of several of these qualified ingots, using the nominal depletion voltage V_p (voltage required to deplete to a carrier density of 10^{16} cm^{-3}) resulting from a representative Se implant as the test parameter. This is typically more sensitive than the profile depth. Figure 2.1-1 contains a plot of depletion voltage obtained vs slice number in the ingot; uniform behavior is found over most of the ingot, with a slow decrease in V_p towards the tail, as might be expected on the basis of Cr segregation effects and thre observed distribution of Si. The uniformity of V_p was also evaluated across an entire slice 2.3 inches wide by 1.6 inches high; these results are shown in Fig. 2.1-2. The standard deviation (obtained after omitting points within 3 mm of the edges) was 130 mV. Within

Table 2.1-2

Variations Along Ingot Length of Si Concentration in Crystal Specialties GaAs Ingots (from SIMS analysis)

Ingot	Front	Si Concentration (cm^{-3})	Electrical Behavior
XS3787	Front	6E15	Qualified
XS3787	Tail	1E15	Qualified
XS4033	Front	1E16	Unqualified
XS4033	Tail	5E15	Qualified
XS4572	Front	8E15	Qualified
XS4572	Tail	5E15	Qualified
XS4639	Front	1.2E16	(undoped-n type)
XS4639	Tail	6E15	(undoped-n type)
XS4643	Front	8E15	Qualified
XS4643	Tail	1E15	Qualified
XS4776	Front	1.7E16	Unqualified
XS4776	Tail	2E16	Qualified

the area that would be occupied by the circuit of an IC wafer, the standard deviation was 50 mV. The variations in pinchoff voltage around the mean also appear to reflect effects of segregation (the facet of the growing crystal does not coincide with the plane of the slice). The results indicate a degree of uniformity within the limits required for fabrication of SDFL circuits. A possible avenue for further improvement of uniformity is to increase the melt size (from the current neighborhood of 1000 gm) inasmuch as this would spread the segregation effects over a larger volume of GaAs.

Additional research efforts have been carried out at Crystal Specialties under the current program to improve ingot yield. Ingots were grown with a moderate increase (x2) in the amount of Cr added to the melt in order to decrease the percentage of ingots that fail to qualify at the seed end. Preliminary indications suggest that this may be a successful technique. Coating of

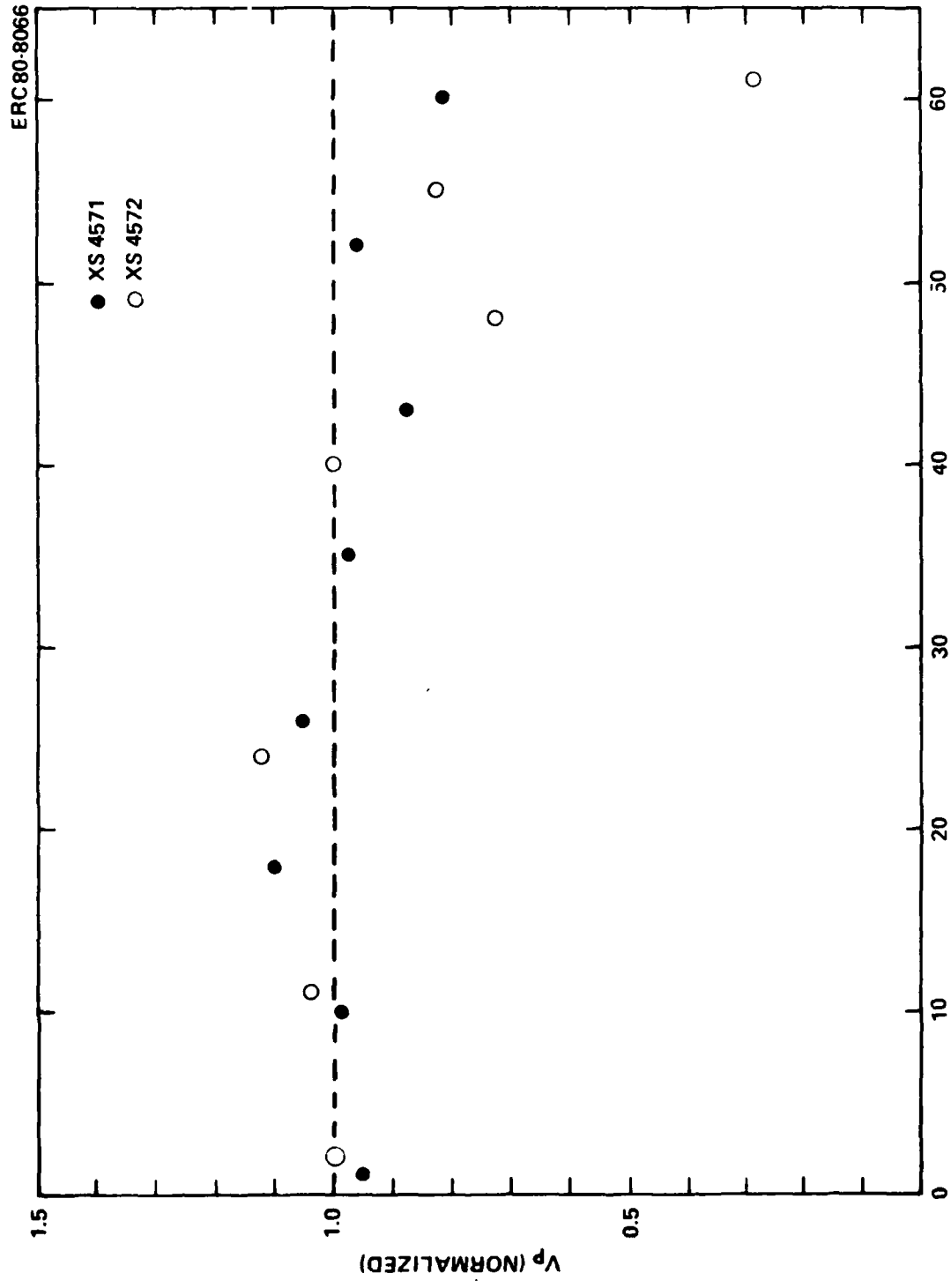


Fig. 2.1-1 Uniformity of Se implant along ingot length of two Bridgman ingots.

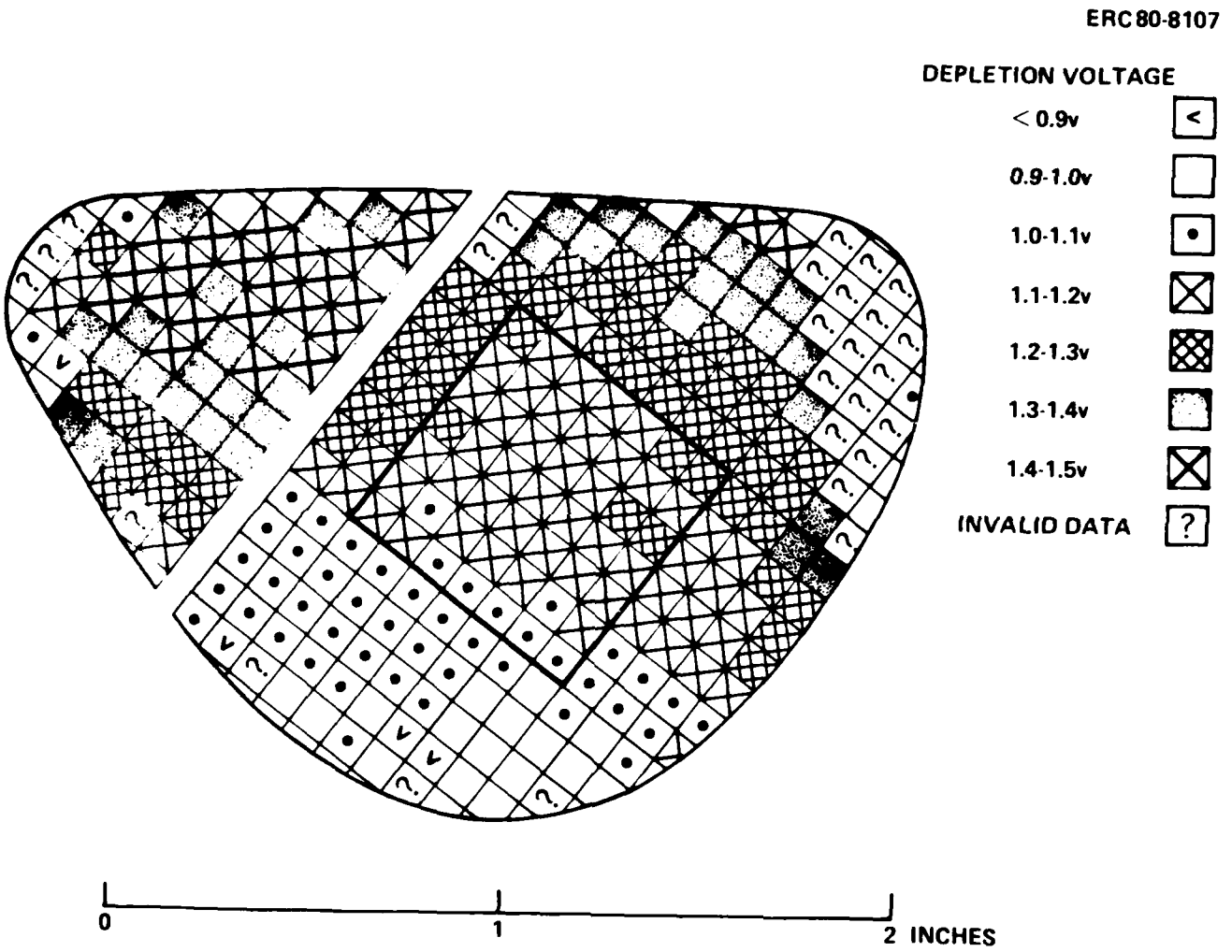


Fig. 2.1-2 Uniformity map of entire slice of Bridgman material indicating variations in depletion voltage. The square outline indicates the area that would be occupied by an IC wafer.

quartz growth boats with a layer of Si_3N_4 also has been carried out. The Si contamination during growth in such a coated boat did not appear to be reduced; however, the use of both a coated boat and a coated ampoule remains to be attempted. Boat coatings may also be of benefit in reducing boat-wetting, which has been a recurrent problem in the Bridgman growth, periodically causing twinning or polycrystalline growth.

Investigations were conducted on the deep levels present in the Bridgman material using a spectroscopy technique based on photoinduced current transients (PITS). A wide variety of levels were found and cataloged. Many levels coincide with previously reported GaAs traps; others, however, appear to have been identified for the first time. GaAs samples from different manufacturers were found to have different characteristic trap spectra. Recent results, obtained with the DLTS technique (under an IR&D program), indicate that the trap concentrations are significantly reduced in the region of the implant during the post-implant anneal, through a mechanism yet to be determined.

During the contractual period, significant improvements were made in the crystal growth facilities at Crystal Specialties, Inc. These include the installation of a clean room for the ampoule loading phase of the process, a cryopump for ampoule evacuation and a gas manifold arranged to allow baking-out the starting Ga material in a Pd-purified H_2 ambient. These improvements did not produce a dramatic step-change in the yield of single crystals grown or in the fraction of ingots qualified for ion-implantation, although it is believed that they have contributed to the long term improvement of these yield values.

2.2 LEC Material

In the past several years a new generation of LEC equipment has been developed to improve the capability for growing III-V materials. Capitalizing on this development, a Metals Research Czochralski puller has been installed and is now in operation at ERC. Recent developments have permitted in-situ synthesis of GaAs in this equipment and have eliminated the separate synthesis of GaAs prior to single crystal growth. The Liquid Encapsulated Czochralski (LEC) method has been specially useful in developing larger ingot sizes suitable for

large area wafers for higher device yields and lower process costs. Recent success in the growth of (100) oriented ingots offer round wafer shapes suitable for automatic process equipment. Although LEC crystal growth and characterization are carried out under IR&D, a brief discussion of this work is included here for completeness in view of the impact on IC fabrication the LEC material is expected to have.

High degree of control over stoichiometry in the LEC process have resulted from the high pressure technology developed for GaP growth. New crystal weighing methods have been developed to permit in-process diameter control in GaAs resulting in diameter uniformities competitive with silicon. Components of the Czochralski system can be prebaked in final assembly to drive off undesirable volatile impurities prior to starting a growth cycle. A cold wall system allows the more volatile impurities to be trapped and removed from contact with the active crucible. The choice of crucible materials is independent of crystal growth considerations, and dependent only on the chemical compatibility, available purity, and mechanical properties.

Control over melt-solid interface regions in the large LEC systems offers the opportunity for optimization of thermal geometries necesary for controlled crystal growth. Resistance heating is a necessity with the growth of large diameter GaAs. Poor thermal conductivity in GaAs can allow strain to develop in the growth of large crystals to the point where the boules actually crack, especially in RF heated pullers where sharp thermal gradients are present. Resistance heating produces more gradual thermal gradients that allow annealing of the as-grown crystal.

Bulk semi-insulating GaAs grown by LEC methods have shown the appropriate properties for application in ion implantation. Both undoped and Cr doped semi-insulating ingots have qualified for use in implantation processes. The electrical properties of undoped and Cr doped LEC semi-insulating GaAs ingots grown at ERC are shown in Table 2.2-1. The sheet resistances of the semi-insulating material as grown and following high temperature annealing are nearly identical within a factor of 2. All of the ingots show isolation resistance well in excess of the IC specification (10^7 Ω/□). Characterization of the LEC

Table 2.2-1

Semi-Insulating GaAs Grown by LEC Technologies at ERC (IR&D Data)

Sample No.	Sheet Resistance Ω/□ As Grown	Sheet Resistance Ω/□ After Anneal*	Se Implant Profile** Data	Crucible	Dopant
R1F	1.6E10	4.2E9	Abrupt, 1.5E17 peak	SiO_2	None
R1T	6.7E9	4.2E9	Abrupt, 1.5E17 peak	SiO_2	None
R2F	6.3E9	3.6E9	Abrupt, 1.5E17 peak	SiO_2	None
R2T	7.7E9	5.0E9	Abrupt, 1.5E17 peak	SiO_2	None
R3F	8.3E9	2.0E10	Abrupt, 1.5E17 peak	SiO_2	Cr
R3T	5.9E9	4.2E9	Abrupt, 1.5E17 peak	SiO_2	Cr
R4F	7.1E9	2.0E10	Abrupt, 1.5E17 peak	SiO_2	Cr
R4T	6.3E9	1.5E9	Abrupt, 1.5E17 peak	SiO_2	Cr
R5F	3.3E9	6.7E9	Abrupt, 1.5E17 peak	SiO_2	Cr
R5T	2.5E9	5.0E9	Abrupt, 1.5E17 peak	SiO_2	Cr
R7F	8.8E8	2.9E9	Abrupt, 1.5E17 peak	PBN	None
R7T	1.1E9	1.0E10	Abrupt, 1.5E17 peak	PBN	None

*1100Å Si_3N_4 cap, 850°C, 39 min, H_2 ambient.

**Se^+, 300 KeV, 3 x 10^{12} cm^{-2}, cap and anneal as in *.

materials by 300 KeV, 3 x 10^{12} cm^{-2} selenium implantation into bare substrates has produced carrier profiles that correspond to LSS range statistics (Fig. 2.2-1) and activation in excess of 80%. Crystals grown from undoped melts have shown similar electrical properties. Also undoped crystals grown from SiO_2 and pyrolytic Boron Nitride are both indistinguishable from Cr doped ingots in character.

Detailed qualification studies such as those described in Section 2.1 have been carried out on ingots 2, 3, 4 and 5. All of these ingots passed the isolation qualification test. In Fig. 2.2-2, C-V profiles from ingots 2, 4 and 5 illustrate the results of the Se profile tests. In all cases the shape of the profile corresponds very well with what is expected for qualified semi-insulating material (as illustrated, for example, by the profile from Crytal Specialties ingot XS4643 shown in the solid line in the figure). No indication of the form

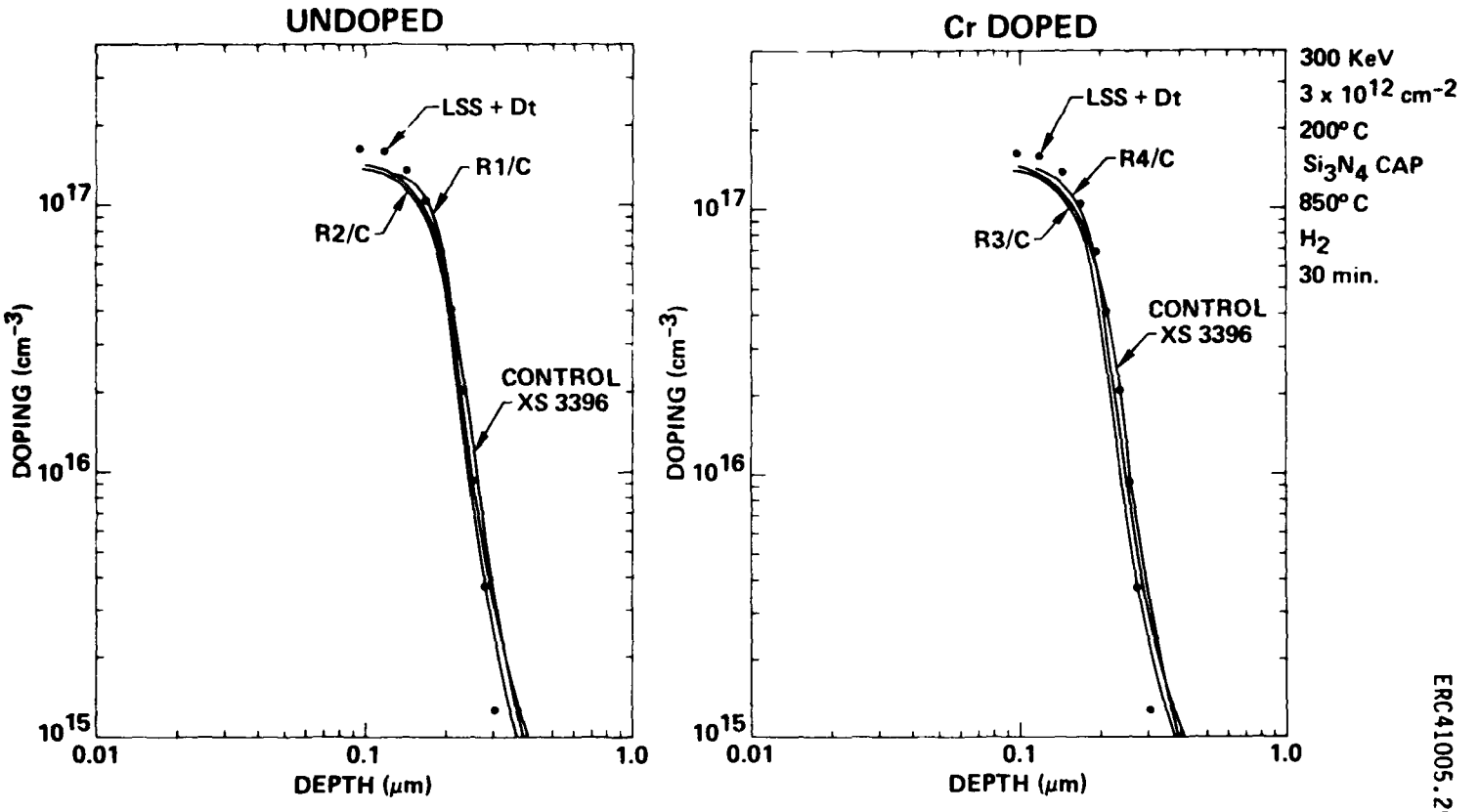


Fig. 2.2-1 Carrier concentration profile for selenium implanted LEC semi-insulating GaAs. (IR&D Data)

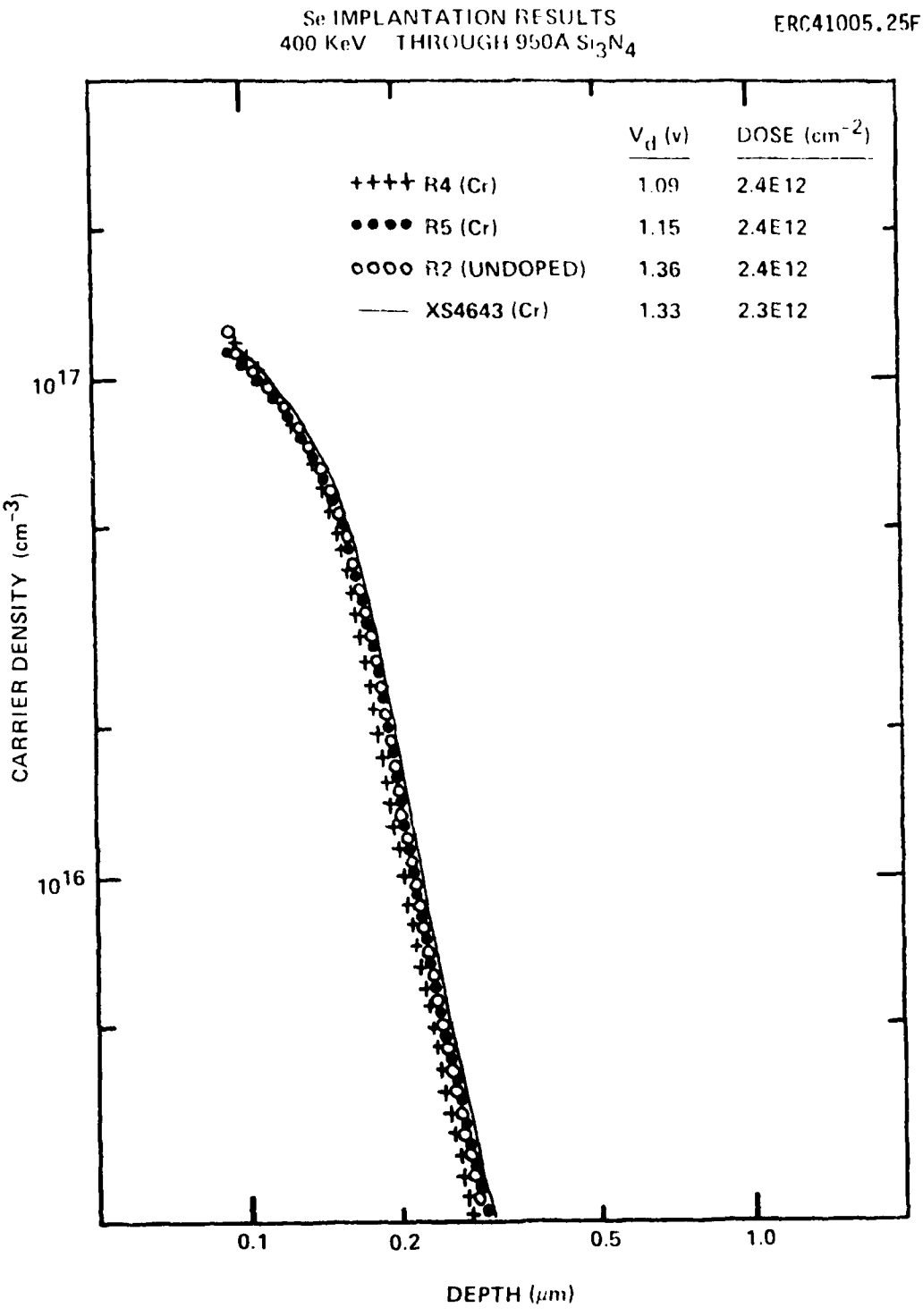


Fig. 2.2-2 Comparison of carrier concentration profiles for 400 KeV implanted Se through 950A Si_3N_4 into three LEC samples (undoped and Cr doped) and a Crystal Specialities Bridgman grown substrate. (IR&D Data)

ation of "deep tails" in the carrier density profiles has been seen. The effective activation of the Se appears to be slightly lower in the LEC material than in the Bridgman material. This is evidenced by the slightly lower values found for the depletion voltage, although the Se dose was 4% larger. The magnitude of this difference is sufficiently low that it should not affect SDFL circuit fabrication, although it should be studied further from the standpoint of determining the nature of the differences in compensation mechanism between Bridgman and LEC substates. Initial studies comparing (111) and (100) wafer characteristics as manifested through Se profiles have also begun, as well as examination of uniformity across large slices. The uniformity of depletion voltage, V_d, evaluated over an entire slice of ingot R5, is illustrated in Fig. 2.2-3. The standard deviation of V_p in the best quadrant was only 45 mV. Chemical analysis of LEC crystals has been performed by Secondary Ion Mass Spectrometry for both common donor, acceptor, and deep level impurities. Results of such analysis by SIMS are compared with those from Cr doped GaAs grown by the horizontal Bridgman method (XS4033) in Table 2.2-2. The LEC materials show lower concentrations of Si than the Bridgman material. Boron oxide used as an encapsulant in the crystal growth process acts both as a diffusion barrier and gettering agent for those elements which form stable oxides (e.g., Si, Mg, etc.). It is interesting to note the low Si concentration in the LEC crystals is consistent with the hypothesis relating the high background doping of horizontal Bridgman growth with melt contamination from SiO_2.

2.3 Wafer Flatness and Substrate Preparation

In order to achieve the LSI/VLSI densities desired, a high degree of wafer flatness is required for use with projection mask aligners capable of achieving 1 μm resolution. The Canon 4X mask aligner used at ERC for IC fabrication imposes a flatness specification of ±1.5 μm/cm for polished wafers. The current IC process requires approximately 1 μm resolution in 1 - 1.5 μm thick photoresist. The next generation 10X mask aligner will have similar wafer flatness requirements; however, it will be equipped with automatic focus and auto align capabilities opening the way for practical fabrication of larger wafers.

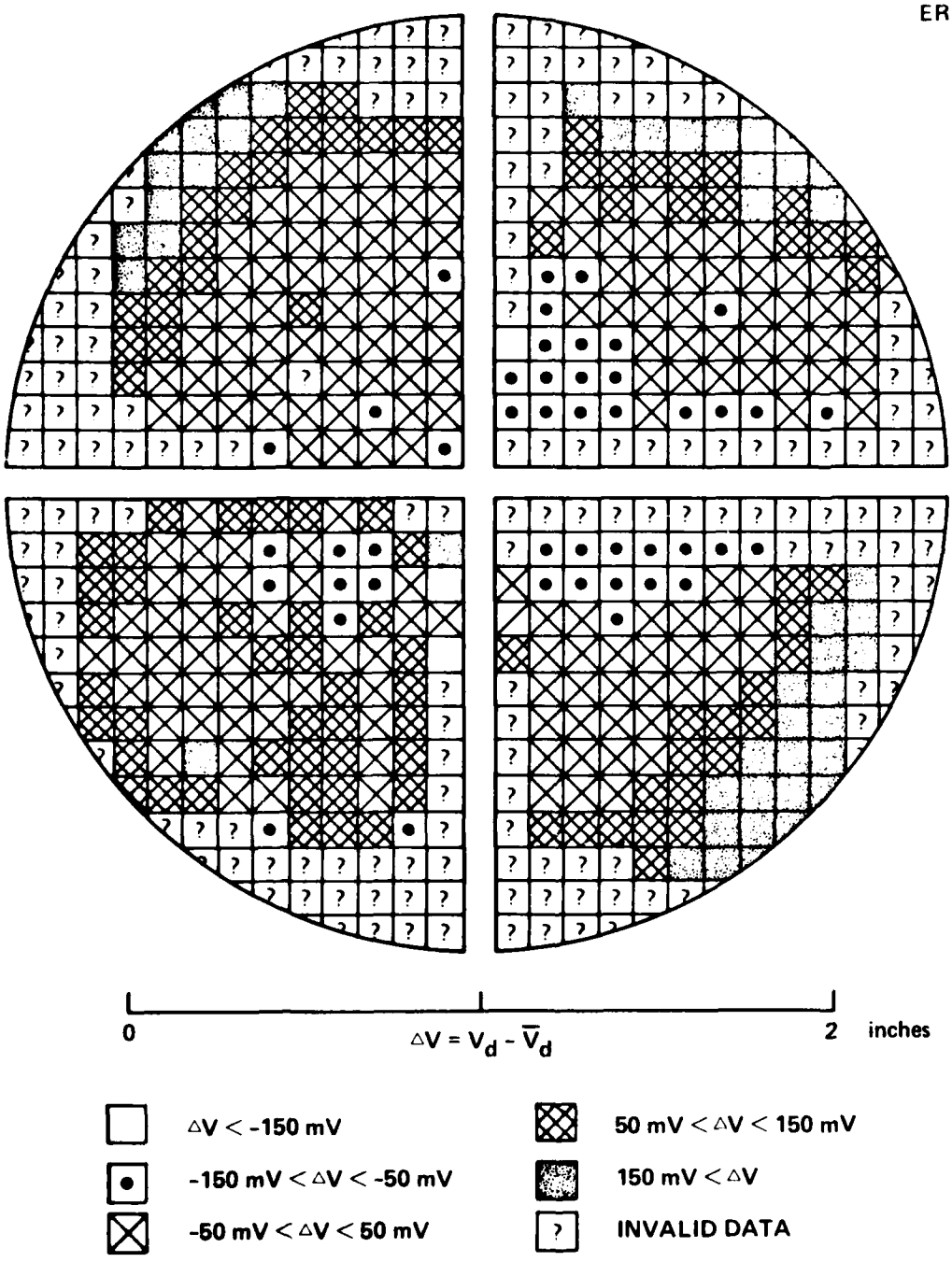


Fig. 2.2-3 Uniformity of depletion voltage from LEC ingot R5, for 400 KeV Se implantation through 950Å Si_3N_4. (IR&D Data)

Table 2.2-2

Chemical Analysis of High Purity Semi-Insulating GaAs by Secondary Ion Mass Spectrometry (in cm^{-3}) (IR&D Data)

Sample	Si	S	Se	Te	Mg	Cr	Mn	Fe	B	
R2F	8.1E14	2.1E15	<E14	<E14	3.1E15	3.9E14	8.6E14	7.2E14	4.2E	14
R2T	1.0E15	2.9E15	<E14	<E14	5.6E15	1.2E15	1.7E15	4 E15	7.0E	14
R4F	6.3E14	1.4E15	<E14	<E14	3.6E15	1.1E16*	1.5E15	1.9E15	1.2E	15
R4T	1.2E15	3.9E15	<E14	<E14	2.8E15	4.8E16*	2.4E15	1.1E15	3.8E	14
R7F	1.3E15	3.2E15	2.4E14	<E14	1.3E15	1.7E14	3.9E14	2.1E15	6.2E	14
R7T	2.4E15	6.3E15	1.6E14	<E14	3.2E15	1.9E14	8.2E14	2.3E15	3.4E	15
XS4033F	1.2E16	1.2E15	2.0E14	<E14	3.9E14	4.2E15*	3.5E14	2.5E15	6.0E	13
XS4033T	4.9E15	4.2E15	6.7E14	<E14	7.2E14	2.0E16*	4.2E14	3.0E15	1.8E	14

*Intentionally Cr doped.

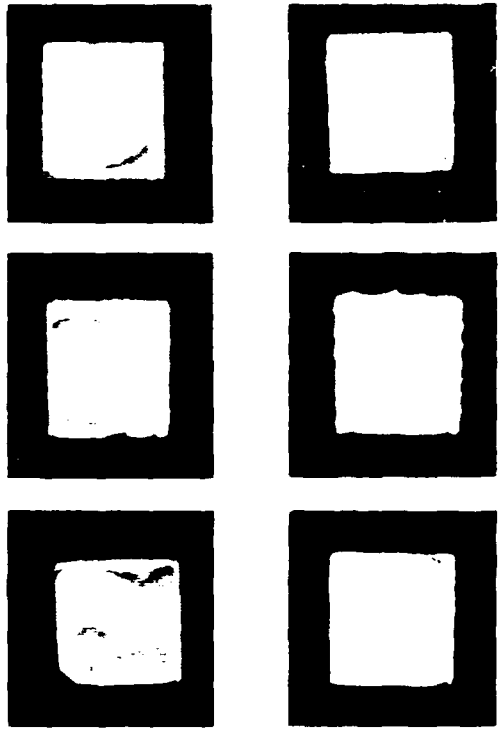
To obtain wafers meeting the ± 1.5 μm/cm flatness criteria, efforts have been concentrated on this area both at Rockwell and at Crystal Specialties. In addition, each processing step is evaluated relative to wafer deformation. This has resulted in substrates which can be successfully used for IC fine line processing.

High degrees of wafer planarity are not easy to achieve. Crystal Specialties has implemented optical polishing techniques such as those used for producing high degrees of flatness in optical components in an effort to improve wafer flatness in the polishing operation. New techniques for holding the wafers on the polishing plate are also under consideration, since wafers apparently polished flat may bow after they are freed from the polishing plate. This is an area of considerable importance, since with the extension to larger wafers flatness over greater areas will be required.

Since wafer deformation is related to wafer thickness, rather thick, 0.025 inch substrates are used as the standard starting material. Careful polishing by vendors and chemical etching of the back side yields flat slices from which the smaller wafers can be cut with the 3 μm specified flatness. The stress induced by the sputtered Si_3N_4 encapsulant produces compressive forces

which result in deformation of the wafer. To counter-balance this stress, a coating of Si_3N_4 is first applied to the back side resulting in a slightly concave front surface. The wafers are then given a final cleaning and polish prior to the application of Si_3N_4 to the front side. Flatness photos illustrating the high degree of flatness achieved on the 1" × 1" square wafers used in IC processing are shown in Fig. 2.3-1. Chemical etching in GaAs is anisotropic due to the differential etch rates for the high index planes. To create a less preferential etch rate, a chem-mechanical process employing bromine-methanol was selected for polish damage removal. The resultant surface finish is featureless, and the flatness is nearly identical to that observed initially except for some edge rounding.

Experiments have been undertaken to explore the possibilities for balancing the stresses emanating from Si_3N_4 deposition by reversing the above procedure and tailoring the back Si_3N_4 thickness to compensate for bowing caused by the front side Si_3N_4, deposited first in this case. Initial studies have provided positive indications for this technique; however, more investigation will be done to evaluate the technique before implementation in the process.



AS POLISHED

AFTER BACKSIDE Si_3N_4

AFTER FRONTSIDE & BACKSIDE Si_3N_4

0.5 μm/FRINGE

Fig. 2.3-1 Flatness monitor photos illustrating wafers after polish after backside Si_3N_4 deposition and frontside Si_3N_4 deposition. Each fringe represents a 0.5 μm variation in flatness.

3.0 ION IMPLANTATION

As a vital part of the planar GaAs IC process, ion implantation continues to be the subject of intensive study. During the current program, studies have been undertaken on a number of important topics relating to the successful application of implantation. In the following sections, results and future directions for implantation research in GaAs are highlighted. Among the topics discussed are: n-type doping studies, including Cr redistribution phenomena (Section 3.1); Si ion implantation for n^{++}, n^-, and n^+ layers (Section 3.2); recoil effects from implanting through the cap (Section 3.3); crystal orientation effects (Section 3.4); and low temperature annealing effects (Section 3.5).

3.1 N-Type Doping Studies

The reproducibility of the ion implanted n^- layer for FET channels is critical to the fabrication of high performance LSI/VLSI circuits since the characteristics of this layer have a direct effect on the pinchoff voltage and saturation current of the FETs. In this program, significant advances have been made toward understanding the behavior of the n^- implants and applying this knowledge to process technology. Studies on uniformity and reproducibility were undertaken. In addition, the role of Cr diffusion during the post-implant anneals in controlling electrical characteristics was identified and characterized.[2-4]

Through SIMS measurements (carried out by Charles Evans and Associates) it was found that the Cr content of the GaAs substrates undergoes redistribution during the post-implant anneal, leaving a region several microns deep depleted of Cr (see Fig. 3.1-1a). By profiling a sample through the Si_3N_4 cap (as shown in Fig. 3.1-1b) it was determined that virtually all of the displaced Cr accumulates at the cap-GaAs interface. Although the measured concentration of Cr near the GaAs surface is typically found to be $3 - 5 \times 10^{15}$ cm^{-3}, a comparison with SIMS profiles under identical conditions on GaAs samples known to be essentially Cr free indicates that most or all of this perceived Cr concentration is due to

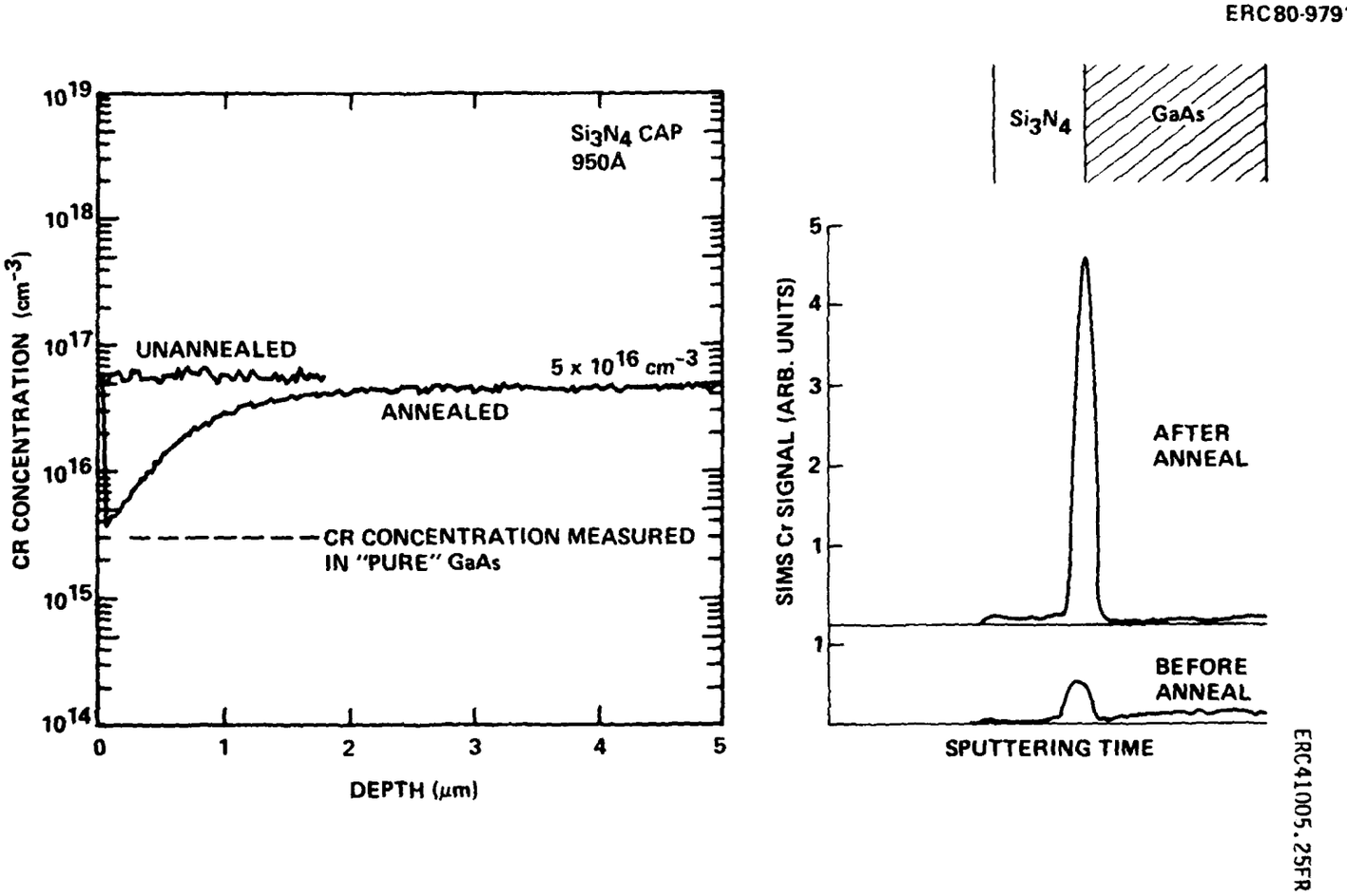


Fig. 3.1-1 Cr distribution after anneal (850°C 30 min) SIMS profile.

background effects in the measurement, and that the actual Cr density is reproducibly reduced to below 10^{15} cm^{-3} near the GaAs surface. The electrical effects of the Cr motion were explored, both in unqualified and qualified substrates. It was determined that the depletion of Cr leads to undercompensation of residual donors present in the material as illustrated in Fig. 3.1-2. If the level of residual donors (principally Si) is excessively high (as in unqualified substrates), an n type layer is formed even without implantation. This n-type layer can lead to isolation failures in ICs; at the same time, deep tails are formed in the carrier density profiles of n^- implants. To confirm this result, detailed comparison were made between Cr and Se profiles (as measured by SIMS), and carrier density profiles measured with the C-V technique in unqualified GaAs substrates. Several such profiles are shown in Fig. 3.1-3 (where the scale is chosen to emphasize the tail region of the implant). Also shown in the dashed line is the profile corresponding to what is expected for the Se implant alone (as determined by a combination of electrical and SIMS measurements). The carrier density didstributions in the unqualified samples are found to consist of the sum of a component due to the Se implant together with a linearly varying excess doping density. The slope of this excess density is in detailed agreement with what is expected on the basis of the measured Cr diffusion coefficient ($\sim 9 \times 10^{-12} cm^2/sec$ at 850°C) and the measured bulk Cr concentration of the substrates as shown in Table 3.1-1.

Table 3.1-1
Bulk Cr Concentration in Unqualified Substrates

Sample	Electrical	SIMS	Growth Data
A	2.2×10^{17}	1.8×10^{17}	1.6×10^{17}
B	5.5×10^{16}	4.2×10^{16}	Not Available
C	1.9×10^{16}	3.8×10^{16}	$\sim 1.9 \times 10^{16}$
D	1.8×10^{16}	2.7×10^{16}	$\sim 1.9 \times 10^{16}$

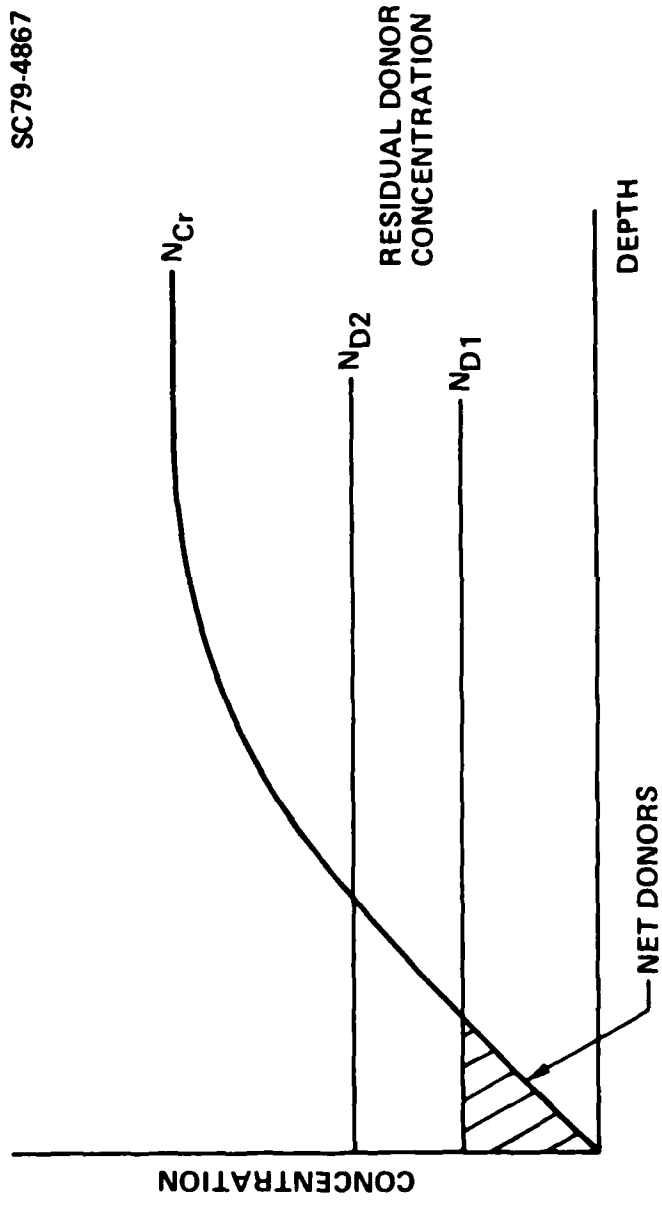


Fig. 3.1-2 Electrical effect of Cr redistribution.

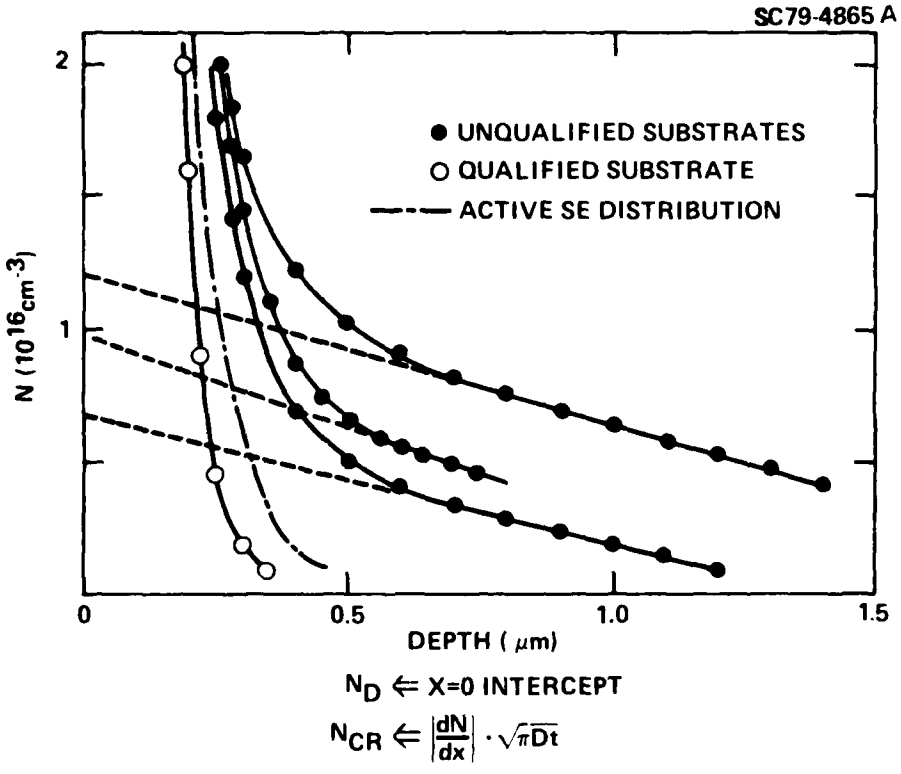


Fig. 3.1-3 Electron density profiles Se implanted GaAs (linear scale).

In qualified GaAs substrates, the undercompensated layer formed by the Cr redistribution is so thin that it is completely depleted at zero bias, and as a result, unimplanted material retains high resistivity. Nonetheless, depending on the density of residual donors, variations may be induced in the carrier density profile resulting from n^- implants. A model was formulated for the observed doping profiles for Se implants. In this scheme, the doping density takes into account the Se concentration, the residual donor density and the redistributed Cr profile in the material. A numerical procedure was developed to include the effect of depletion of the channel from the substrate-channel space-charge region. The resultant calculated profiles are in excellent agreement with experiment (see Fig. 3.1-4).

Experimental observations and the analytical model were used to show that the Cr redistribution phenomenon greatly enhances the reproducibility of the implant results. By reducing the Cr density in the region of the channel layer, the resultant characteristics are made largely independent of the Cr concentration of the substrate, which, due to segregation during crystal growth, can vary significantly over the length of an ingot.

The diffusion characteristics of Cr in GaAs substrates as a function of anneal temperature and capping technology were also investigated. Over the range 750° - 950°C with a Si_3N_4 cap, the Cr diffusion coefficient was measured and an activation energy of 2.75 eV extracted. These results, however, extrapolate to different values than those suggested by experiments of Magee et al.,[5] who have found significant Cr diffusion at lower temperatures. In light of this, it would appear to be important to verify that no changes take place in the Cr distribution as a result of circuit operation over extensive periods or as a result of low temperature annealing. To address this question, samples of GaAs were capped, implanted with Se and annealed at 850°C for 30 min. Subsequently, one of the samples was subjected to an additional prolonged anneal at 230°C for 600 hrs in an effort to observe low temperature redistribution. A comparison between their Cr profiles as measured by SIMS (Fig. 3.1-5) indicated no noticeable difference between them. Similarly, the carrier density profiles measured on the original sample and the one subjected to the prolonged anneal were

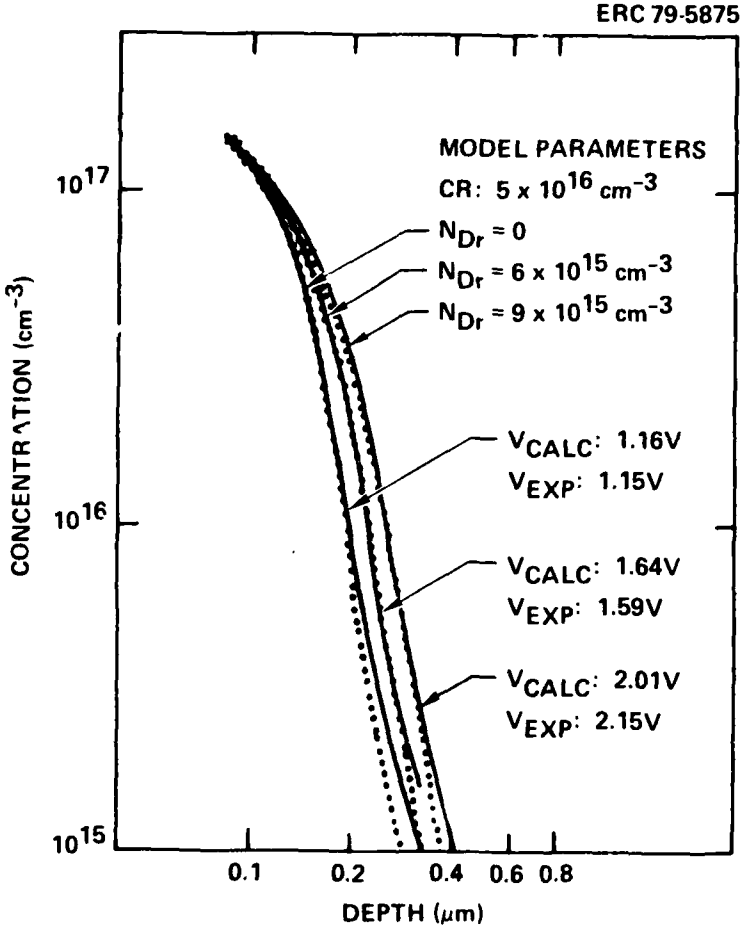


Fig. 3.1-4 CV profiles theory (···) and experiment (——) for Se implants at 400 keV, 2.5 × 10^{12} cm^{-2}, capped.

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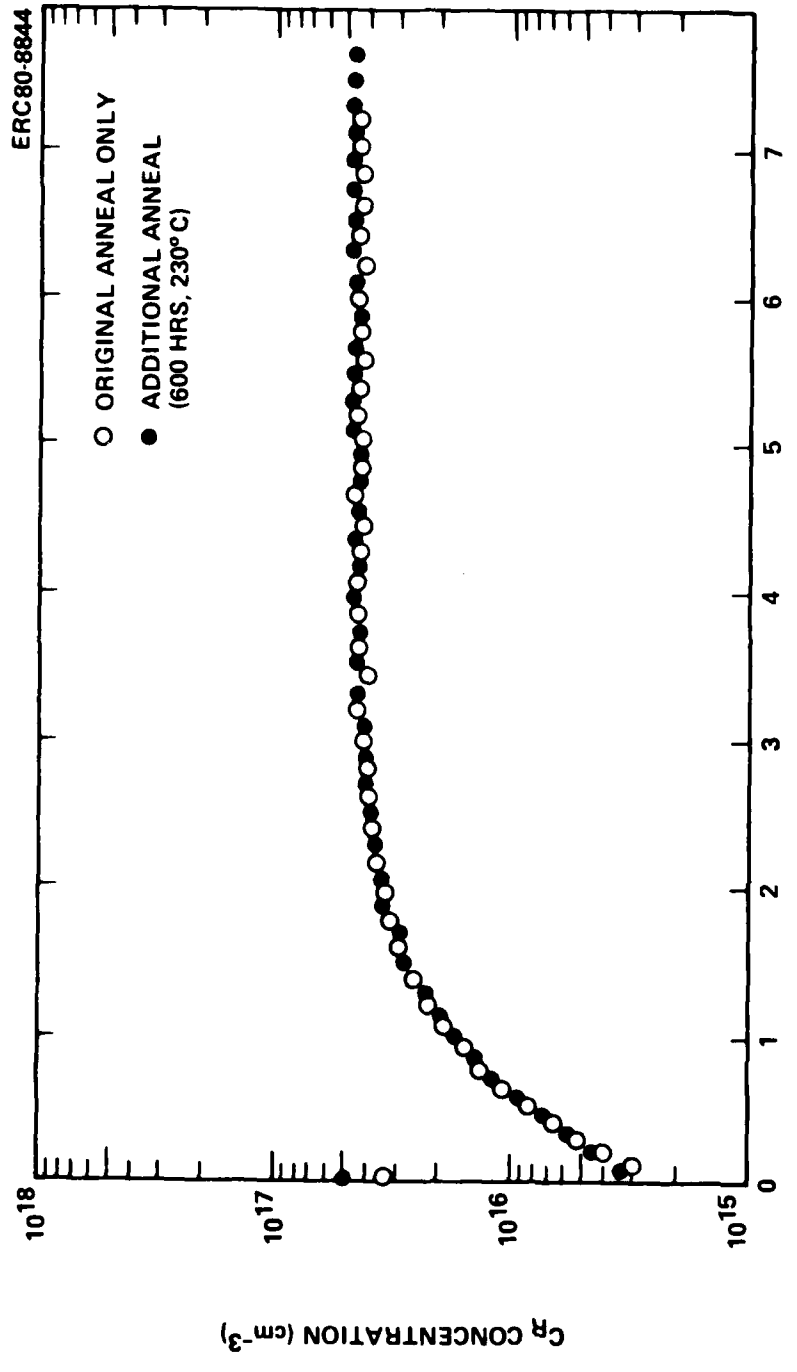

Fig. 3.1-5 Cr concentration profile of a Se implanted layer before and after an extended low temperature anneal.

identical, as shown in Fig. 3.1-6. These results appear to alleviate concerns over the possibility of circuit degradation due to Cr redistribution.

The variations in electron density profiles of n^- implants, particularly in the tail region, remain a subject of interest for the attainment of highly reproducible device results. On the basis of the modeling work, it is believed that these variations will be eliminated if the residual donor densities in the substrate can be reproducibly maintained below $\sim 2\text{-}3 \times 10^{15}$ cm^{-3}. In practice, it has been found that with currently grown Bridgman ingots, reproducible pinchoff voltages can be obtained from Se implants by making slight adjustments in the Se dose used. Theory and experimental results correlate in that the pinchoff voltage obtained is shifted linearly with dose at a rate of approximately 1 V per 10^{12} cm^{-2} (Se, 400 KeV implants). The use of adjustments of this type is made practical by the fact that the substrate characteristics do not vary significantly over the length of a GaAs ingot. Studies have been undertaken on the uniformity across wafers for both Bridgman and LEC material. This is an area needing further and continued attention as material improvements progress and processing requirements increase the demand for uniformity.

3.2 Si Implantation

Another area of development is the investigation of Si implantation for heavily doped contacts and as a possible replacement for both S and Se. Si may offer several attractive features which make it a preferable alternative. Room temperature implantation of Si may activate better and be more reproducible for both channel and contact applications. A more controllable profile may be achieved with less diffusion with Si. In addition, the possibility of using only one implanted species throughout the process is a desirable feature from the point of view of manufacturing.

During the current program, work on Si implantation in Cr doped GaAs was carried out. Studies on heavily doped regions for contacts[6,7] and dual implantation of Si with P and As were carried out in conjunction with Caltech. In addition, work at ERC to evaluate the feasibility of replacing S and Se in the IC process with Si was begun.

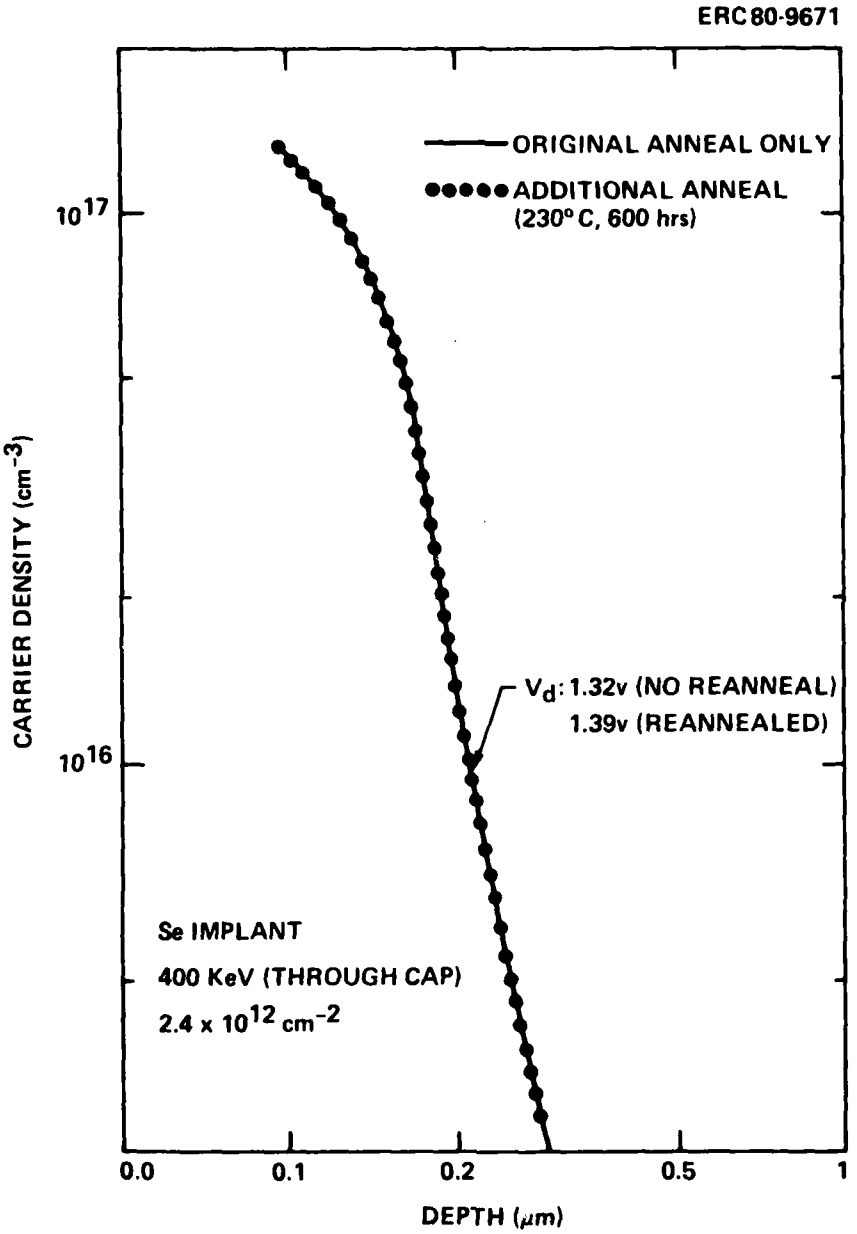

Fig. 3.1-6 Carrier concentration profile of a Se implanted layer after an extended low temperature anneal.

Generally, studies have indicated that it is necessary to carry out high dose implants of group VI dopants at elevated temperatures (approximately 200°C or higher) in order to obtain good activation of the implanted dopant.[6] The processing of GaAs integrated circuits would be simplified if the n^{++} implants, like all the other implant steps, could be carried out at room temperature. Since it was reported that the activation of high dose Si implants is greater for room temperature implants than at elevated temperatures,[7] investigations were carried out to document this result for various implant and annealing parameters.

While investigating highly doped layers, the dependence of the ratio of sheet electron concentration to the implantation dose (N_s/N_D) on anneal temperature (T) with N_d as a parameter was studied (Fig. 3.2-1). For low doses, N_s/N_d was found to approach unity; samples implanted with higher doses showed considerably lower values of N_s/N_d for the same sample temperature. The highest electron activity, about 90%, was obtained for an implanted dose $N_d = 1.7 \times 10^{17}$ cm^{-2} annealed at 900°C for 30 minutes. Sheet resistivity ρ_s vs implantation dose was also investigated and lower values of ρ_s were obtained for the 900°C anneals than for the 800° or 850°C anneals. Ther lowest value, 22.7 ohms/ was encouraging since it is about a factor of two lower than the lowest value reported for Se implants at elevated (350°C) temperatures.

Studies were also made on the shape of the implanted profile for high dose Si implants. Generally, the higher the implanted Si dose and the higher the anneal temperature (for T > 850°C) the flatter and deeper the n_e electron profiles are. Figure 3.2-2 shows the profile calculated for 300 keV, 10^{15} cm^{-2} Si as calculated through LSS range parameters using a Pearson distribution.[8,9] The as-implanted Si distribution, measured by SIMS, is only slightly broader than the calculated profile, but after annealing the Si distribution has broadened considerably. Compared to the atomic Si distribution after annealing, the electron concentration is lower by nearly an order of magnitude, approximately constant over the whole measured depth. Apparently the electron concentration profile is not simply determined by the diffusion of Si, but is also the result

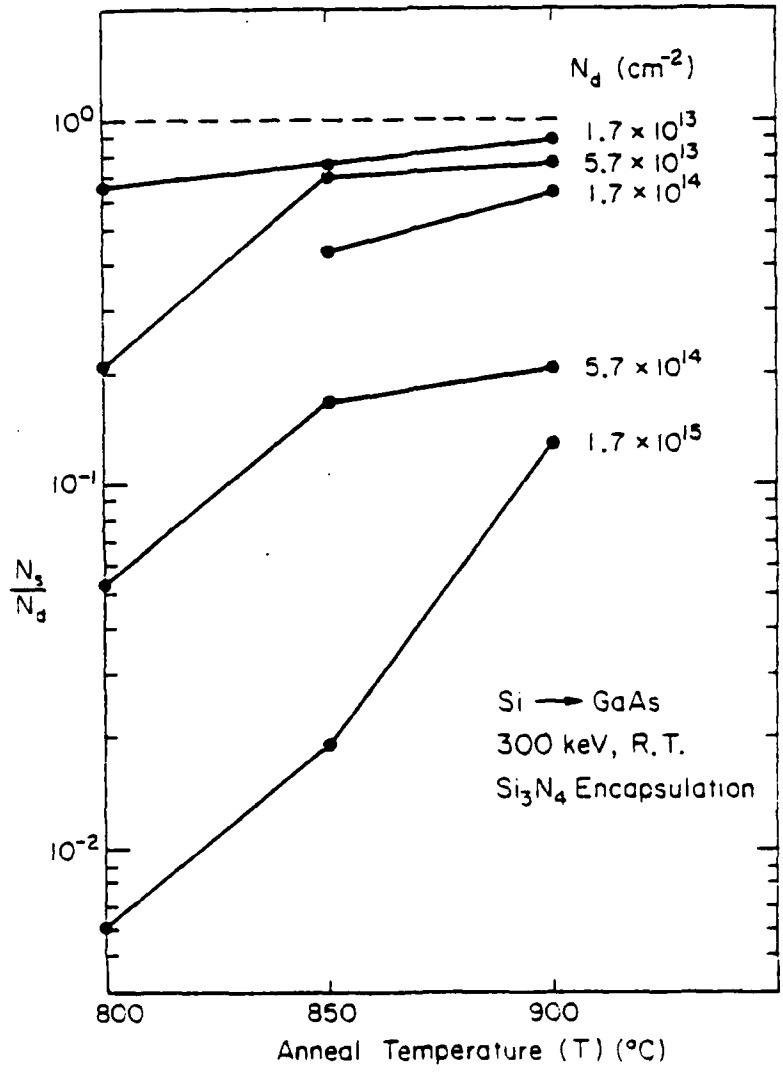

Fig. 3.2-1 Ratio of sheet electron concentration to implantation dose as a function of anneal temperature for Si implanted GaAs.

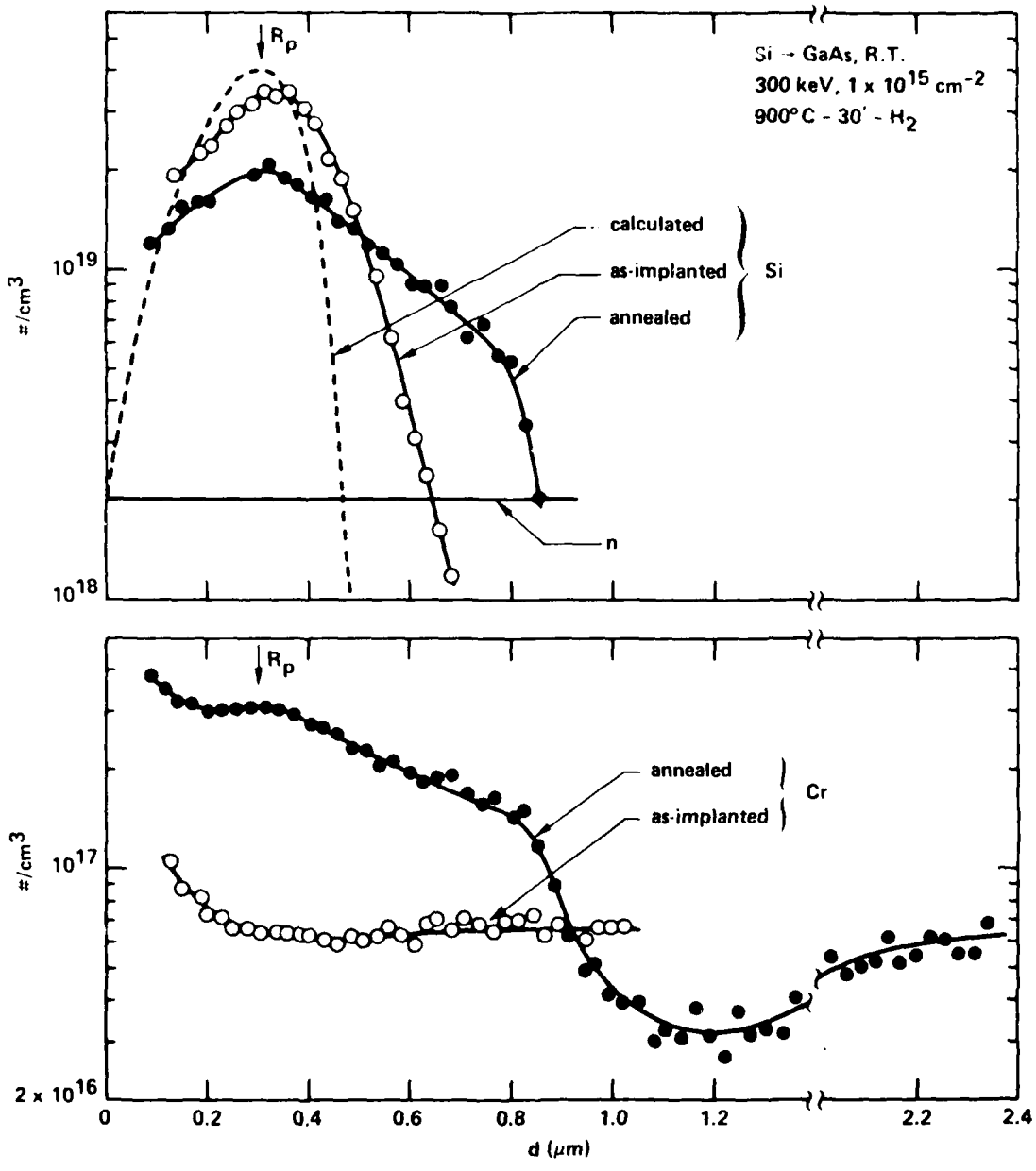

Fig. 3.2-2 Concentration profiles of Si measured by SIMS after room temperature implantation into semi-insulating (Cr-doped) GaAs before and after thermal annealing in a H_2 atmosphere with a sputtered silicon nitride cap. The dashed line is a calculated theoretical distribution for a dose of 10^{15} cm^{-2} Si ions of 300 keV. The straight line indicates the free electron concentration (n).

of incomplete electrical activity. Differential Hall and carrier concentration measurements on samples covering a range of doses confirmed that the electron distribution is always nearly flat at a value of 2×10^{18} cm^{-3}.

In view of the existence of a maximum attainable free electron concentration independent of implanted dose or annealing temperature, double implantations of Si and P were carried out to determine if the electrical activity could be enhanced. Implants of 100 keV Si or Si and P ions (same dose per ion species) were made at room temperature into GaAs substrates. After capping and furnace annealing for 30 min in H_2 at temperatures between 800 and 900°C, initial Van der Pauw measurements indicated that at an implanted dose of $2 \times 10^{13}/cm^2$, the sheet electron concentration, N_s, did not reveal dramatic differences for either single or dual implant conditions. At an implanted dose of $10^{15}/cm^2$, the samples implanted with both Si and P (total dose $2 \times 10^{15}/cm^2$) showed an ~ 50% higher sheet electron concentration than those implanted with 10^{15} Si/cm^2 only. Samples annealed at 850°C reached a maximum of about $6 \times 10^{17}/cm^3$ for a Si dose of 2×10^{13} cm^{-2}, and a maximum of $8 \times 10^{17}/cm^3$ for Si and P doses of 2×10^{13} Si/cm^2, respectively. The maximum net electron concentration expected from LSS range theory for implanted Si of 2×10^{13} cm^{-2} dose, would be $1.8 \times 10^{18}/cm^2$. The electron concentration profiles were rather flat in the first 3000A, the maximum corresponding roughly to the maximum predicted from LSS theory for the atomic concentrations.

In the case of $10^{15}/cm^2$ implants, the maximum electron concentration is $1.5 - 2 \times 10^{18}/cm^3$ for both single- and double-implanted samples, and occurs beyond the LSS range. The mobilities show a behavior similar to that observed in the lower dose implantations. For the doses of Si and P chosen, initial observations did not show a significant change in the free electron concentration due to double implantation. Similar initial results have been observed for dual implantation of As with Si.

Si implantation is a promising method of obtaining electron concentration as high as 10^{18} cm^{-3} utilizing room temperature implantation and annealing at 850°C (the same implant and anneal temperature used for the n^- and n^+ implants). The results of studies with Caltech have indicated the feasibility

of applying Si to the regions of ohmic contact. Further work remains in the area of optimization, actual contact measurements, and the effect of implanting high doses through the Si_3N_4 cap.

In addition to the heavy doping studies, work has been initiated at ERC to begin determination of the feasibility of replacing Se or S with Si throughout the process. Experiments have been run to simulate the type of profile developed with Se and S using Si, with positive results. In addition, test samples were implanted with various isotopes of Si and mass spectra studies have been performed to assure the purity of the Si beam in the 400 keV Extrion implantation system.

For fabrication of FET channel-type layers, Se and Si implants were carried out (in materials which were known to exhibit different degrees of "tailing" on the basis of previous Se implants) for a range of fluences and several energies. The results of these studies have been encouraging. Despite the lighter mass of Si, and therefore larger predicted straggle, the profiles are comparable to those from Se implants, exhibiting approximately the same shape and doping efficiency, as well as a high degree of the activation. An example of the profiles from these studies is shown in Fig. 3.2-3, in which carrier concentration profile froms Se and Si implantations are shown for the same substrate, cap, and anneal parameters. In general, the profiles showed approximately the same or less tailing for Si in ingots characteristically producing variations in profile depth.

SIMS was also utilized to investigate Si implants before and after 850°C, 30 min anneal. Figure 3.2-4 shows that the distribution of implanted Si remains virtually unchanged after anneal. The conclusion reached at this point is that Si is a very suitable substitute for Se in the planar IC process. Further experiments adjusting the dose and energy parameters to optimize the active layer have been outlined.

The use of Si implantation for the diode and contact layers currently formed by S implantation was also investigated. Here, the reprodubility of Si may be a key advantage to its use. Typical results from these initial studies are the curves in Fig. 3.2-5, in which doping profiles of deep Si implants made

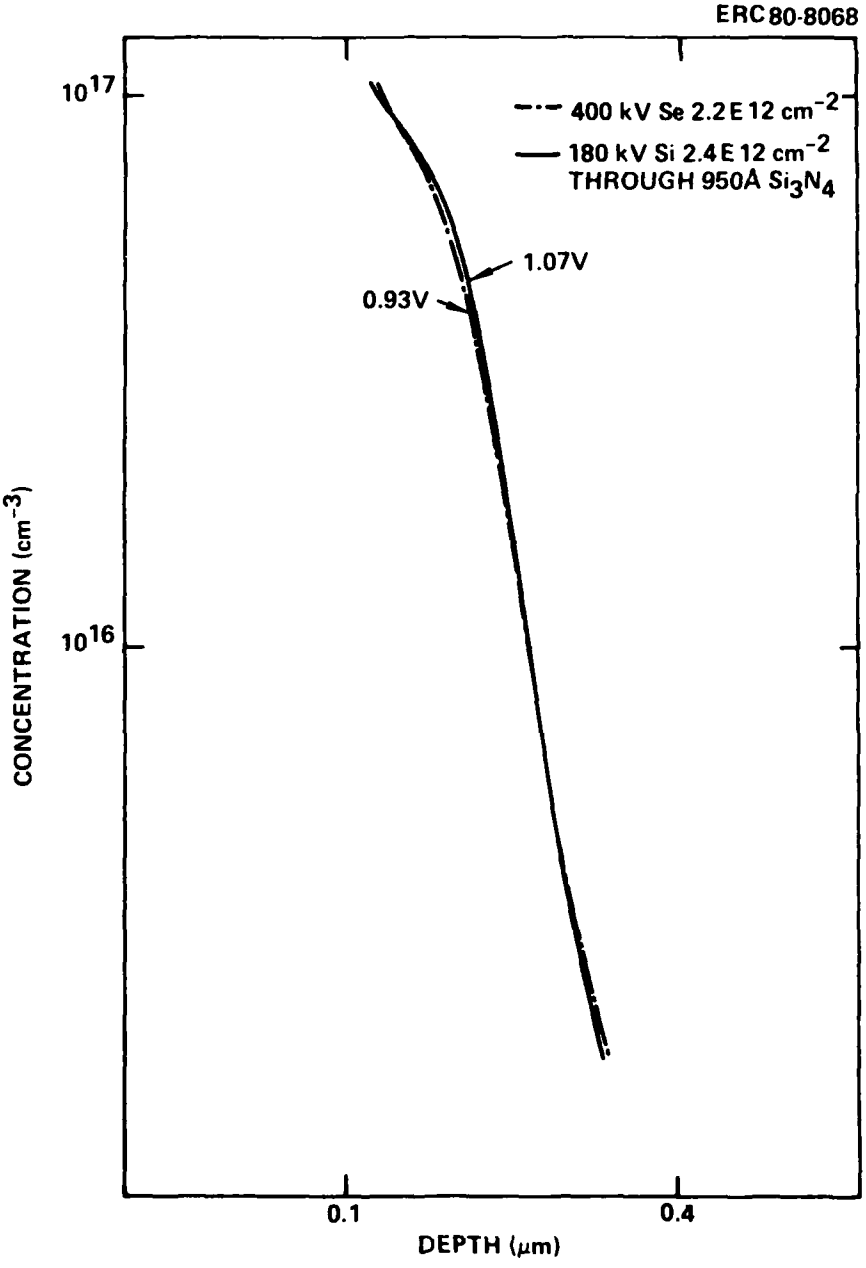

Fig. 3.2-3 Carrier concentration profiles for Si and Se implants through 950Å Si_3N_4, annealed at 850°C for 30 minutes.

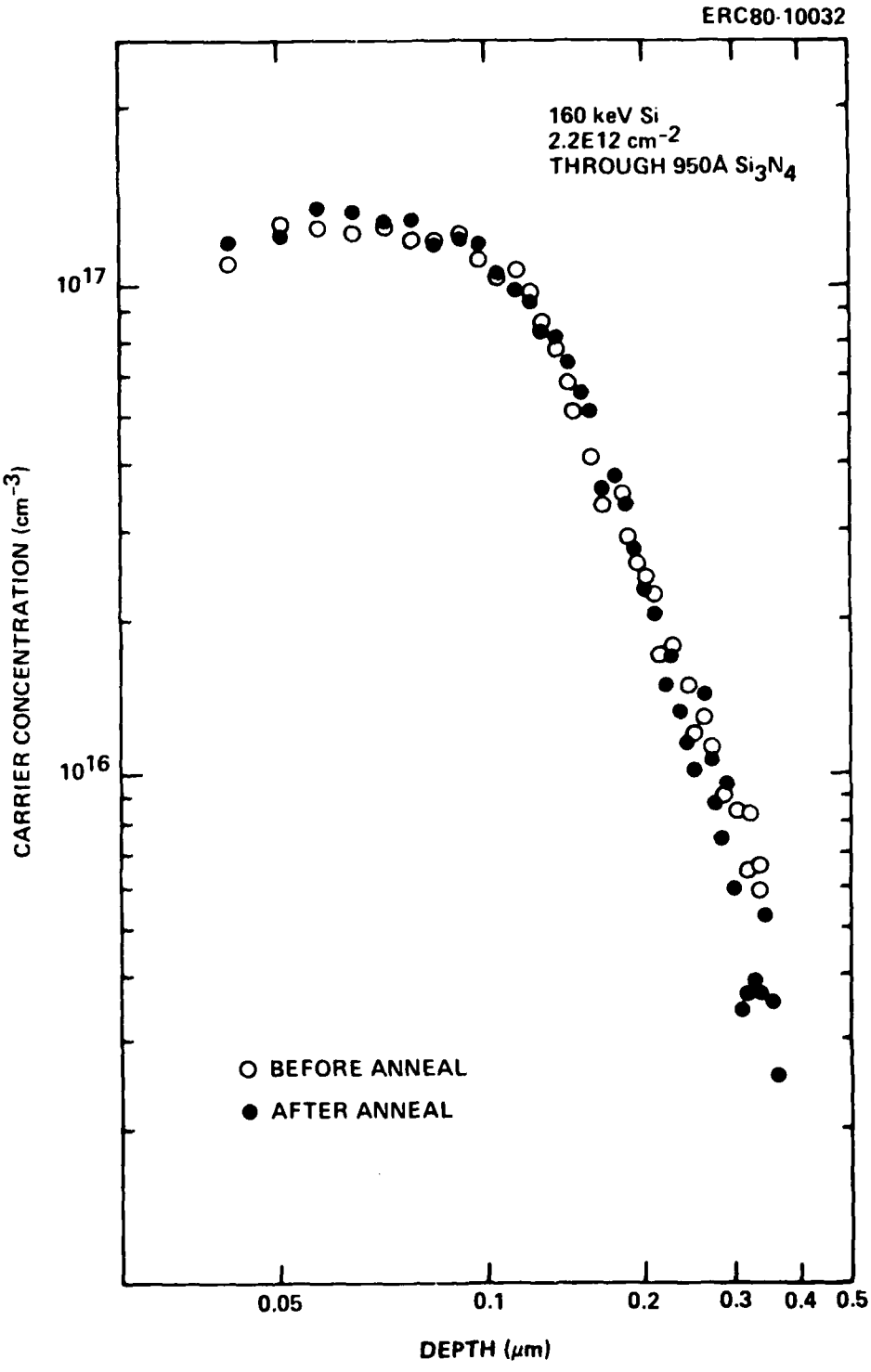

Fig. 3.2-4 SIMS profiles for implanted Si before and after 950°C anneal.

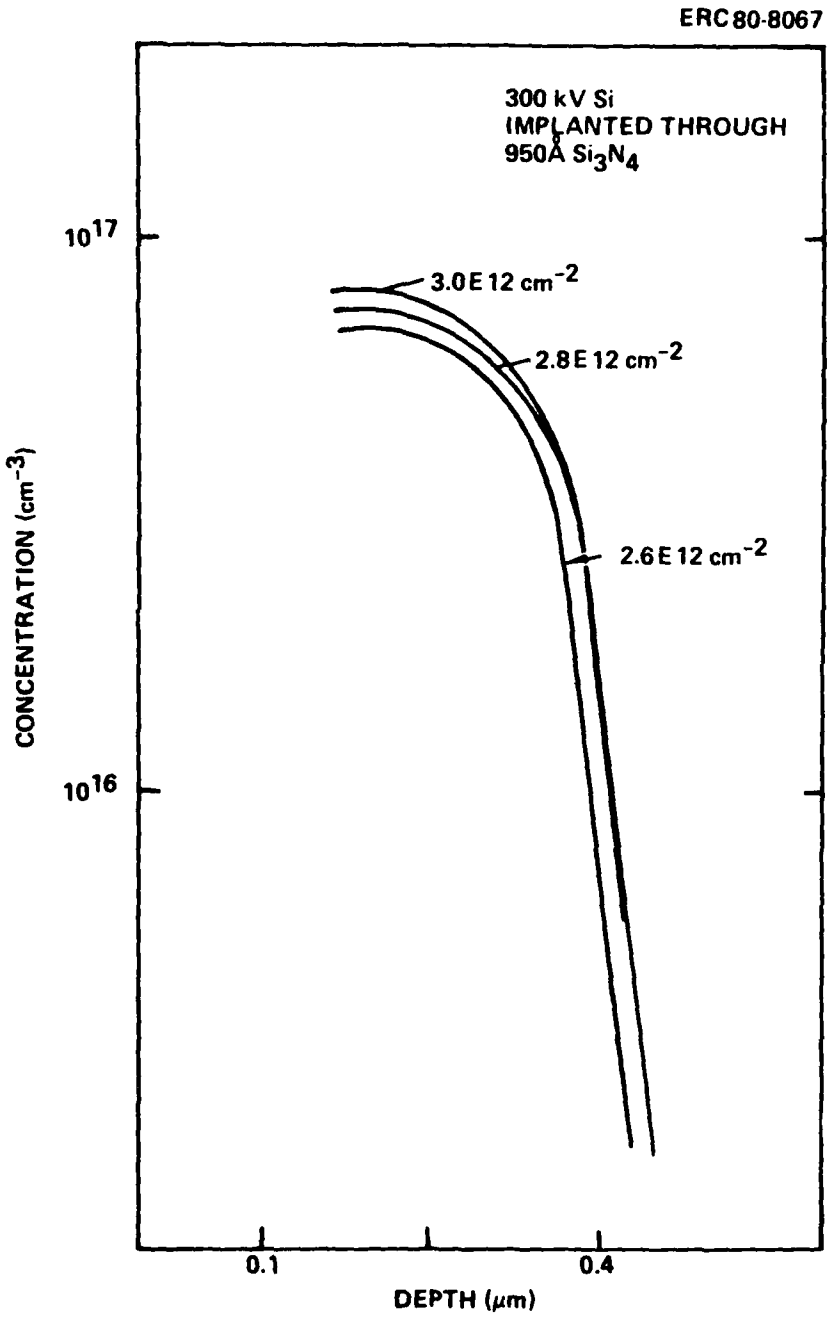

Fig. 3.2-5 Carrier concentration profiles for 300 kV Si implants through 950Å Si_3N_4 annealed at 850°C for 30 minutes.

through 950Å of Si_3N_4 are shown. The depth and height of the profiles track well the increases in fluences and energy and give indications of good reproducibility, and good activation.

In summary, during the current program, preliminary studies indicate the feasibility of moving to an all Si process. Further studies remain to fully evaluate and optimize Si implantation and better characterize its possible advantages.

3.3 Recoil Studies

Although no direct evidence for concern about the possibility of recoils resulting from implantation through Si_3N_4 has been observed at ERC, this area is being investigated to determine possible effects on the type of implanted profiles utilized in the IC process. Relatively little work has been reported in the literature on this important subject. Studies have been undertaken in collaboration with J. Gibbons and Lee Cristel of Stanford, where Boltzman transport calculations for implants through Si_3N_4 are being carried out.[10] Experiments have begun at ERC to compare the results of theoretical predictions with fabricated layers.

In the initial experiments, both electrical and SIMS data were analyzed for low fluence (2.5×10^{12} cm^{-2}) implants of Se and Kr both on bare substrates and through a 950Å Si_3N_4 cap. In addition, N was implanted to determine possible effects from nitrogen knock-ons in the material. These studies were directed toward determining whether the presence of tails in Se profiles might be due to the presence of Si atoms recoil-implanted into the near surface region of the GaAs substrate. The results from the calculations of Gibbons and Cristel, illustrated in Fig. 3.3-1, indicated that at these low fluences, Si knock-ons may be present to a considerable depth into the sample. If electrically active, these Si ions would contribute to the carrier concentration profile ostensibly produced by Se ions, resulting in a tail. The preliminary studies showed no definite indication of the effect of recoil Si in the electrical data.

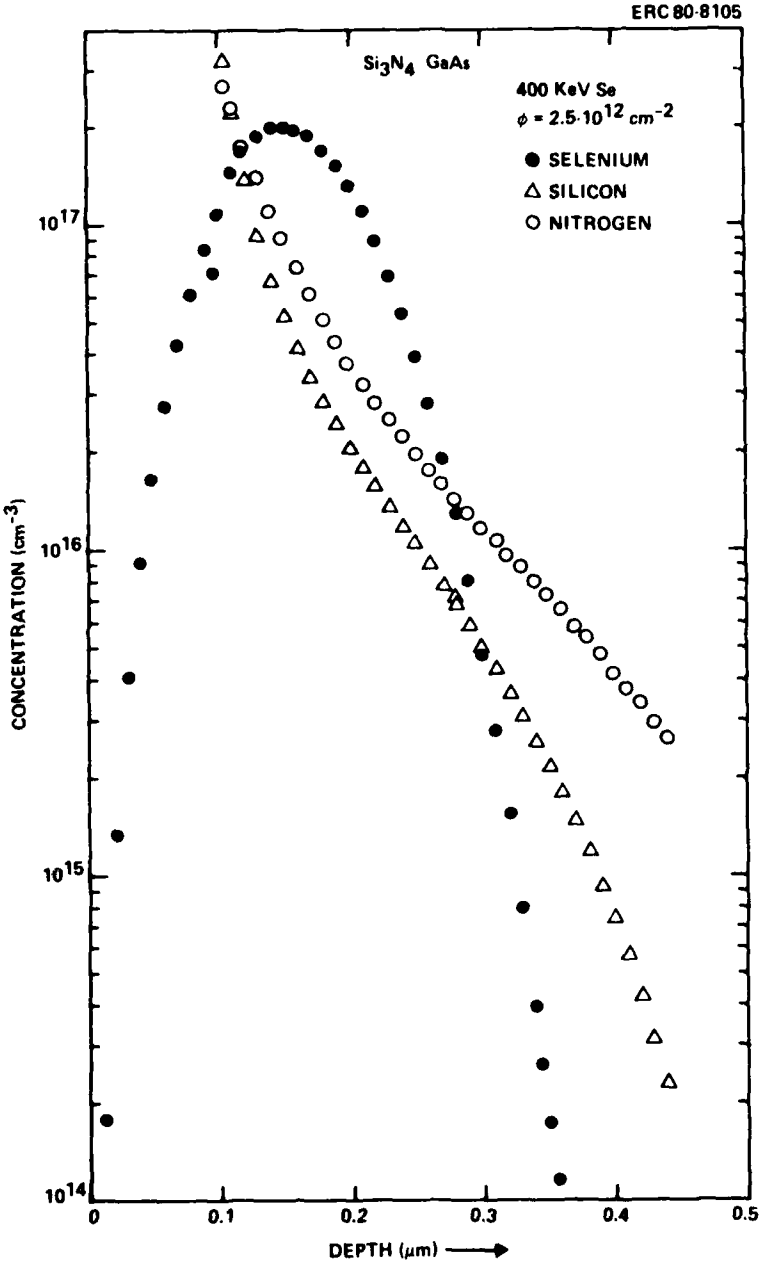

Fig. 3.3-1 Calculated profiles for atomic distribution of recoil Si and N for 400 keV Se implanted through 1000A Si_3N_4 (from Gibbons and Cristel).

Carrier density near the surface of undoped (n type) GaAs substrates after capped and bare Kr implants (380 keV, 2.5 × 10^{12} cm^{-2}) and subsequent annealing was investigated. The calculated Si profile, if 100% electrically active, would induce a change of about 0.6 V between the voltages required to deplete Schottky barriers to a fixed depth (0.3 μm for convenience) on materials capped before and after the implant. The average shift, shown in Fig. 3.3-2, was quite small compared to this predicted figure with error bars due to fluctuations in the background carrier density.

Si was observed near the surface in the SIMS measurements; however, it appeared to be likely due to residual Si from the Si_3N_4 rather than a recoil effect. The sensitivity of the SIMS technique dictates the use of high fluence through Si_3N_4 implants to produce a definite observable effect. Unfortunately, at these fluences, the electrical measurements become unwieldy due to poor dopant activation. However, in order to observe the effect and test the efficacy of the theoretical calculations, further SIMS studies are presently in progress utilizing high fluence bare and through the cap Se and Kr implants so that the knock-on Si can be reliably profiled and compared to Gibbons and Cristel's calculations for these parameters.

For high dose experiments, undoped (100) GaAs samples from Crystal Specialties were encapsulated with 950A of silicon nitride. Control samples were also prepared without an encapsulation layer. Both capped and bare samples were implanted with either 400 keV Se or 400 keV Cr, to fluences of 2 × 10^{14} or 2 × 10^{15} ions/cm^2. After implantation, the silicon nitride was removed from the encapsulated samples and all samples received a gold evaporation. Atomic concentration profiles were measured with SIMS by Charles Evans and Associates.

The profiles resulting from these studies show close resemblance to the theoretical calculations. In Fig. 3.3-3, data for Se and Si profiles are shown for through cap implants. The data for 2 x 10^{14} cm^{-2} were shifted up by a factor of 10 for comparison purposes. The background concentration of Si has not been subtracted from these profiles, limiting the range visible for low dose implants. The controls were free of surface Si accumulation except for recoils possibly resulting from contamination due to diffusion pump oil in the 2 × 10^{15}

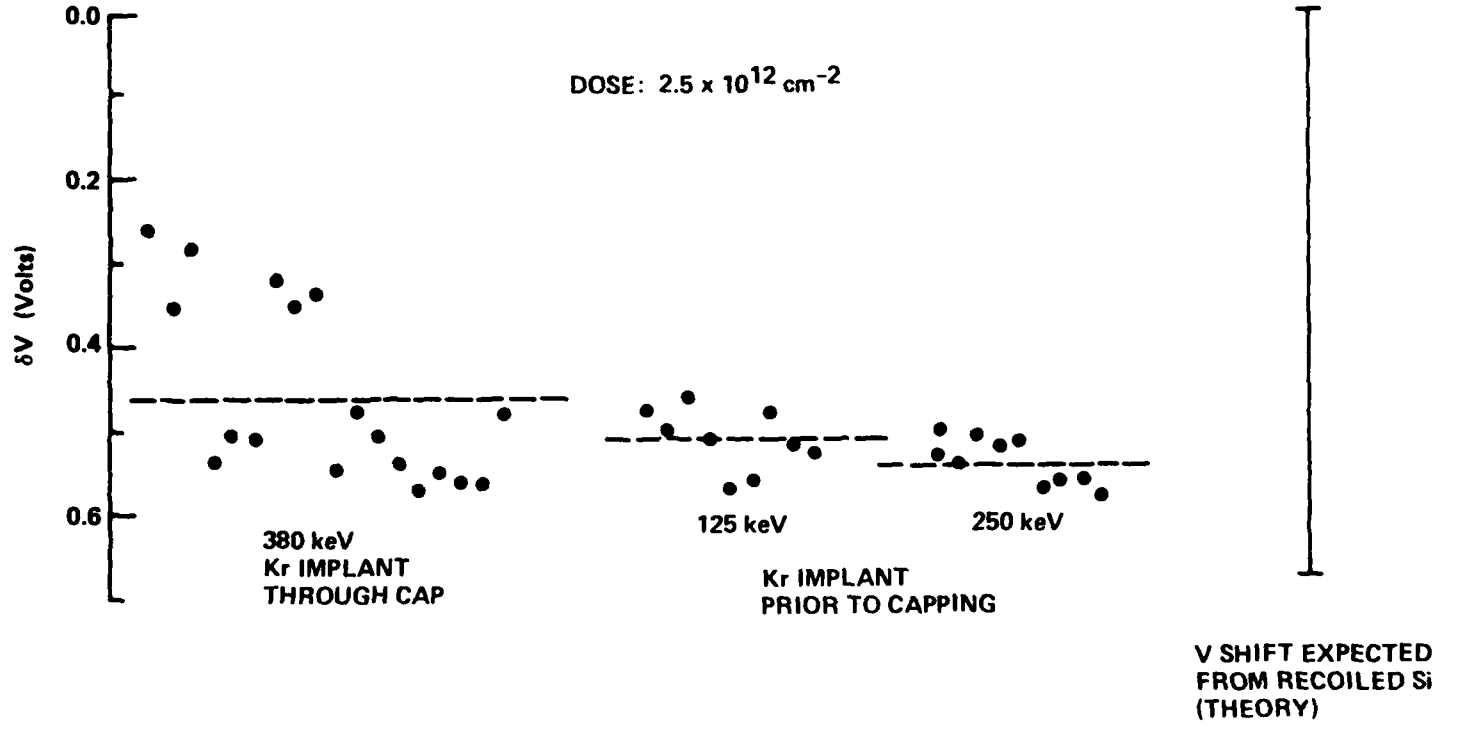

Fig. 3.3-2 Variation voltage required to deplete Schottky barriers to 0.3 μm.

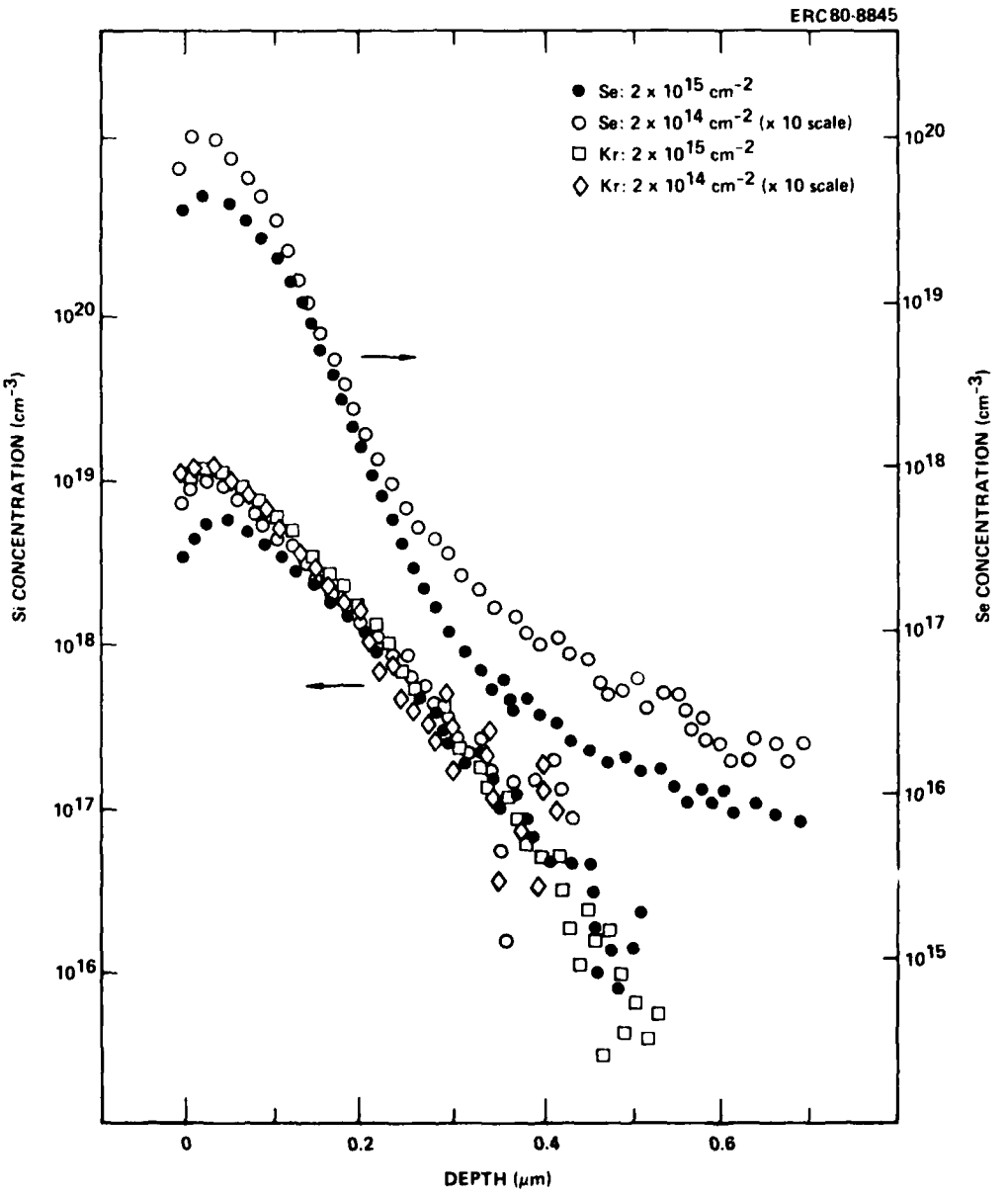

Fig. 3.3-3 SIMS profiles for high dose implants through a Si_3N_4 cap.

cm^{-2} Se implant. Plots for the calculations and experiments correlate quite well, except for the behavior close to the surface, and the absolute concentration.

The measured concentration profiles drop rapidly near the surface because the samples were coated with a layer of gold prior to profiling. The use of the gold successfully avoided spurious Si signals that appeared in earlier low dose work, probably due to dirt or incomplete Si_3N_4 removal.

Features close to the surface are lost due to limitations in SIMS resolution (of the order of 300A) arising either from crystal surface irregularities, ion mixing or cratering effects. Another technique problem is the uncertainty in the location of the cap-GaAs interface. The HF etchant used to remove the cap was found to attack the amorphous GaAs formed during implantation, so that it was hard to determine the etch end point. It is estimated that the samples may be overetched by < 250A.

The predicted and measured absolute concentrations differ by a factor of about 2 - 2.5. The Si calibration was done in reference to the As secondary ion count rate, with the proportionality factor determined by a Si implant profiled during the same session under similar sputtering conditions. The Se calibration was similarly obtained, by refering to the 2×10^{15} cm^{-2} bare Se implant. An a priori estimate for calibration accuracy is within a factor of 1.5 - 2. The principal calibration problem is sample charging, which can vary between samples and may affect secondary ion yields differently for different elements. Anomalous Se counts have also typically been found near sample surfaces, possibly due to chemisorbed oxygen. Thus, while the SIMS results tend to suggest that the number of recoiled Si atoms is slightly lower than calculated, the accuracy of the calculated concentrations is not disproven.

Evidence of recoiled N was also found in the SIMS measurements (by monitoring the GaN^- molecular ion). The resulting count rate was, however, noisier, and there is not as consistent a picture of the N profile as there is for Si when comparing the results from all samples. The N calibration factor is uncertain at the moment; a reference implant will be measured.

In summary, recoil studies have been initiated to study the phenomenon and its potential effects, although these effects have not yet been manifest in results obtained through IC processes. Low fluence electrical studies (in the range used for IC work) did not indicate a contribution from recoiled components of the dielectric cap in carrier profiles. For high fluence SIMS studies revealed a correlation between observed and predicted Si recoil profiles. The indication thus far is that the recoiled Si is present but it is not electrically active in sufficient numbers to produce a discernible feature in the tail region.

3.4 Orientation Effects

In the course of studies of electrical characteristics of GaAs MESFETs, it was noted that two identical FETs oriented in two different directions on a (100) wafer may have different pinchoff voltages (V_p) and saturation currents (I_{DSS}).[11] Low pinchoff voltage FETs were fabricated in four different directions (see Fig. 3.4-1) with the n-type channel under the gate formed by 400 keV Se implantation at a typical dose of ~ 2.2 x 10^{12} ions/cm^2, with an additional S implant under the source and drain to form thicker n^+ regions.

It was found that the FETs oriented in the [011] direction (FET A in Fig. 3.4-1) always had lower V_p and I_{DSS}, while the FETs oriented in the [01$\bar{1}$] direction (FET B) had higher pinchoff voltages and saturation currents. The FETs parallel to the [010] and [001] directions had nearly identical characteristics, their values of V_p and I_{DSS} being between those of the [011] FETs.

It is well known that in GaAs, a zinc-blende crystal, the two [011] directions are not exactly equivalent while all the [100] directions are identical. While this property has been used to explain crystallographic properties, the effect on device performance has not been previously reported. Bulk GaAs, a cubic crystal, is electrically isotropic. At the interface between GaAs and the Si_3N_4 annealing cap, however, the anisotropy between the two [011] crystal directions may have an effect on the stresses due to the encapsulation layer. A differential in the stress due to direction may preferentially enhance lateral

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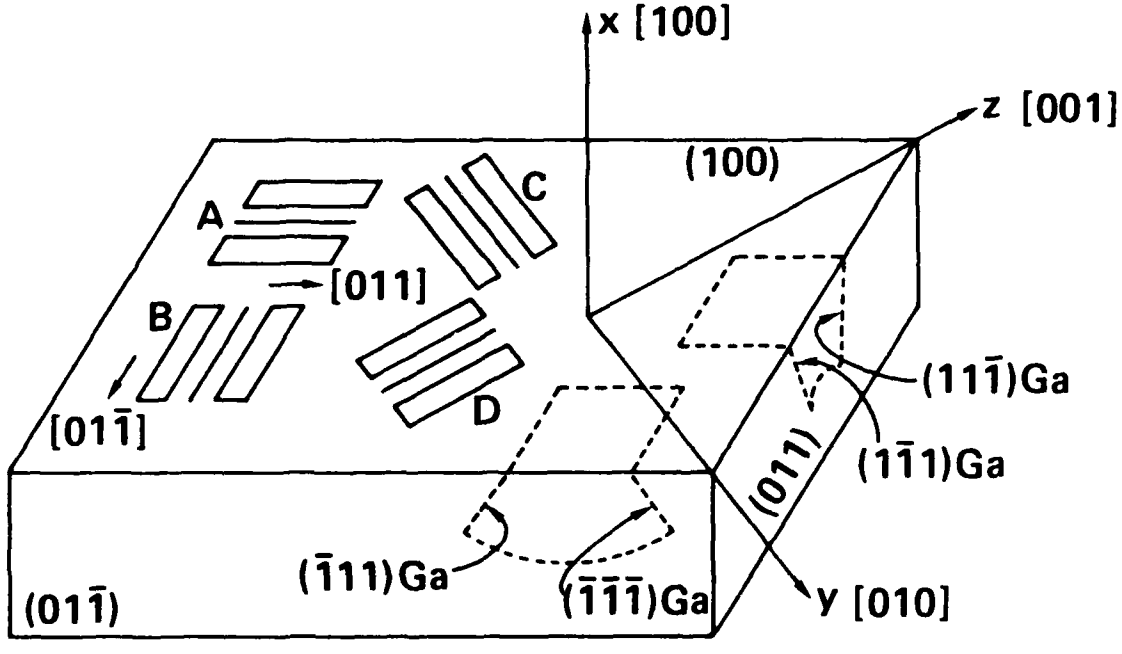

Fig. 3.4-1 Schematic drawing of the orientations of the FETs with respect to the GaAs substrate. A in [011] direction, B in [01$\bar{1}$] direction, C in [010] direction and D in [001] direction. The shapes of the eteched grooves in two different [011] directions are shown by the dashed lines. The differences in the etched pattern enables us to identify the two different [011] directions.

diffusion for the [011] case of the dopant S, which is known to diffuse during anneal,[12] in one direction more than another. Diffusion into the channel would affect the pinchoff voltage and saturation current, causing them to increase. A supporting observation for the lateral diffusion hypothesis was the data indicating that the difference between FET characteristics in the [011] and [01$\bar{1}$] directions was large for short gates and became smaller for longer gates.

A practical conclusion from these experiments is that the FETs must all be oriented in the same direction on a wafer for uniformity of pinchoff voltage. To understand the causes for the orientation effects, studies verifying lateral diffusion phenomena have been undertaken. Among them, is examination of the difference in stress in the cap for the two different directions. Preliminary studies indicate a differential in the stress may be observable. Another avenue is to try to directly observe the lateral diffusion in the channel through a technique such as induced current with a scanning electron microscope. A third related subject for study is the examination of (111) material to determine if it shows similar effects and whether advantages may lie with the use of this particular orientation.

3.5 Low-Temperature Regrowth of Ion Implanted Layers in GaAs (Caltech)

Ion implantation followed by solid-phase epitaxial regrowth is of considerable interest as a technique for introducing n-type impurities into GaAs. It has generally been found that best electrical activity is achieved when the substrate is held at temperatures of a few hundred degrees centigrade during the implantation. The best crystal quality and electrical activity are usually obtained after furnace annealing at temperatures above 600°C. However, it has recently been shown that under certain circumstances good crystal quality can be achieved with implantations at room temperature and below, followed by annealing at relatively low tempertures (180 - 400°C).[13] Williams and coworkers[13] employed relatively low energy implantations (30 - 100 keV) of light ions (< 40 amu) in relatively low doses (< 2×10^{15} cm^{-2}). To attempt to clarify how this processing leads to the observed good low-temperature regrowth, investigation of the parameters that may govern the extent of damage in ion-implanted GaAs and the crystal quality following low-temperature furnace annealing were initiated.

Semi-insulating <100> wafers of Cr-doped GaAs all from the same ingot, were implanted with Si^+, S^+ and Ar^+ ions at energies of 60, 80 and 100 keV, respectively, to doses of 10^{14} - 10^{16} cm^{-2}. Substrate temperatures during implantation were -196°C, 27°C, and 100°C. In addition, As_n^+ molecules with energies of 60 (n = 1, 2, 4) and 180 (n = 1) keV were implanted to similar doses, and with similar substrate temperatures. Samples were annealed without encapsulation at 400°C in flowing dry argon. They were analyzed by backscattering spectrometry of 1.5 MeV He^+ ions channeled in the <100> direction, and detected at scattering angles of 125° and 105°, the latter for improved depth resolution. Quantitative estimates of crystalline disorder before and after annealing were derived from the areas of the disorder peaks after applying a correction for dechanneling. Peak areas in samples that had undergone identical processing differed by no more than 4%.

The results of measurements after implantation and after the longest anneal times are summarized in Table 3.5-1. Considering first the results for as-implanted samples, there is considerable variation in the extent of the implantation-induced disorder from one implant ion species to another. This is illustrated in Fig. 3.5-1 with spectra from samples implanted at room temperature with Si^+, S^+ and Ar^+ ions, each to a dose of 10^{14} ions cm^{-2}. The implantation energies were chosen so that the ion ranges and range straggling were approximately the same ($R_p \sim 700A$, $\Delta R_p \sim 450A$). And yet, the disorder within the region near the surface clearly increases with ion mass. This is indicated by the backscattering yields from these regions. Such yields range from those typical of fairly good single-crystal for the Si (28 amu) implantation to that of amorphous material (i.e., the channeling yield is at the random level) for the Ar (40 amu) implantation. Implantations of these three ions at -196°C all produced amorphous layers, but they showed a similar trend in that the amorphous thickness increased with increase of the ion mass. This behavior is attributed to a primary amount of radiation damage which increases with the mass of the implanted species and an annealing process which depends on the sample temperature. Such annealing is significant at room temperature, but decreases rapidly with decreasing substrate temperature during implantation, as is illustrated in Fig. 3.5-2. The spectra in this figure were obtained from samples implanted at different temperatures with 100 keV Ar^+ to a dose of 10^{14} cm^{-2}.

Table 3.5-1

Summary of Implants and Results of Backscattering Analyses

	Implant			As Implanted		As-Annealed	
Ion	E (keV)	Φ (cm^{-2})	$T_{substrate}$	Crystal/ Amorphous	Amorphous Thickness (Å)	χ_{min} (%)	Displaced Atoms ($\times 10^{-6}$ cm^{-2})
As_1^+	60	10^{14}	100°C	xtal		defect annealing	
As_2^+	60	10^{14}	100°C	xtal			
As_1^+	60	10^{14}	R.T., LN_2T				
As_2^+	60	10^{14}	R.T., LN_2T	am	~ 500	10	2.7
As_4^+	60	10^{14}	100°C R.T., LN_2T				
As_2^+	60	$5x10^{14}$	R.T.	am	600	13	4.1
As_2^+	60	10^{15}	R.T.	am	600	18	5.3
As_2^+	60	10^{15}	LN_2T	am	650	26	7.2
Si^+	80	10^{14}	R.T.	xtal		defect	anneal.
S^+	80	10^{14}	R.T.	xtal		defect	anneal.
As_1^+	120	10^{14}	R.T.	am	830	36	10.8
As_1^+	120	10^{14}	LN_2T	am	860	35	13.6
Ar^+	100	10^{14}	100°C	xtal		defect	anneal.
Ar^+	100	10^{14}	R.T.	am	~ 900	regrowth from surface	
Ar^+	100	10^{14}	LN_2T	am	1050	46	17.0
Si^+	80	10^{15}	R.T.	am	1100	53	20.5
S^+	80	10^{15}	R.T.	am	1100	46	19.0
As_1^+	180	10^{14}	R.T.	am	1100	43	20.0
Si^+	80	10^{16}	R.T.	am	1350	57	27.7
Si^+	80	10^{15}	LN_2T	am	1550	51	30.5

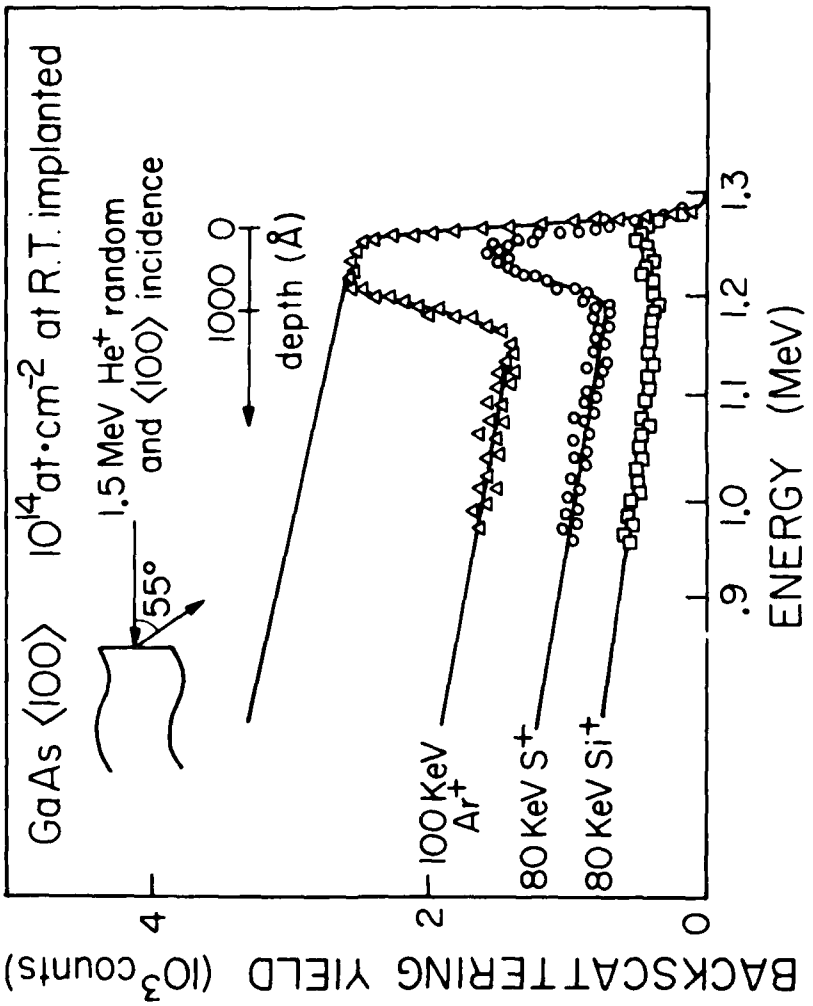

Fig. 3.5-1 Backscattering energy spectra of 1.5 MeV He^+ recorded with <100> incidence for GaAs implanted at room temperature with 10^{14} at. cm^{-2} of Ar^+, S^+ and Si^+.

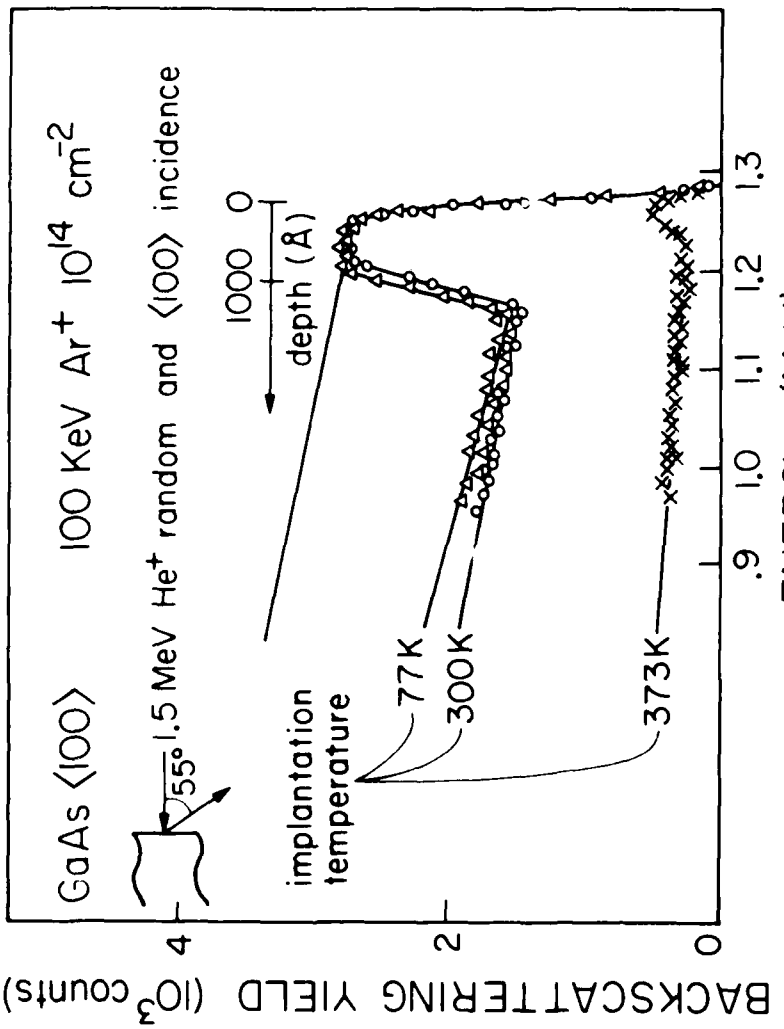

Fig. 3.5-2 Disorder profiles for GaAs implanted with 100 keV Ar^+ to 10^{14} at.cm^{-2} at different substrate temperatures.

Turning to the results for annealed samples, it was found that crystal quality after annealing depends strongly on the state of the material after implantation. In fact, it is convenient to consider the different annealing behavior of three distinct states after implantation. First, if a full amorphous layer has been formed, there is regrowth from the crystal/amorphous interface. Second, if the implantation causes amorphization but leaves a thin layer of single-crystal on the surface, there is regrowth from both sides of the amorphous layer. Finally, when the implantation causes only partial disorder, the heating causes annealing of defects.

For annealing of samples in the first state (fully amorphized layer), it was found that the parameter of primary significance is the thickness of the amorphous layer. To a first approximation, layers with the same initial amorphous thickness exhibit the same residual disorder after annealing regardless of the ion species, dose and implantation temperature. This is demonstrated in Fig. 3.5-3, where the areas of the disorder peaks (which are proportional to a number of displaced atoms/cm^2) after 60 min furnace annealing at 400°C are plotted against the amorphous thickness. The thickness of the amorphous layer was determined from channeled backscattering spectra, and the disorder peak areas were determined from channeled spectra recorded after annealing, assuming a linearly rising background beneath the peak, as indicated in Fig. 3.5-4. Points are included for all of the samnples that were fully amorphous after implantation. The fact that all data points fit on a single curve in Fig. 3.5-3 indicates that the thickness of the amorphous layer is the primary parameter of significance irrespective of the ion species, implantation dose or substrate temperature during the implantation. These data clearly establish that the number of residual defects after annealing increases with the initial thickness of the amorphous layer.

From kinetic measurements, it is known that very little further annealing of these samples can occur at this temperature. Gamo et al,[14] also found that regrowth of 720A of initially amorphous GaAs stopped completely after only 15 min of annealing at 300°C. Therefore, it is believed that the dependence

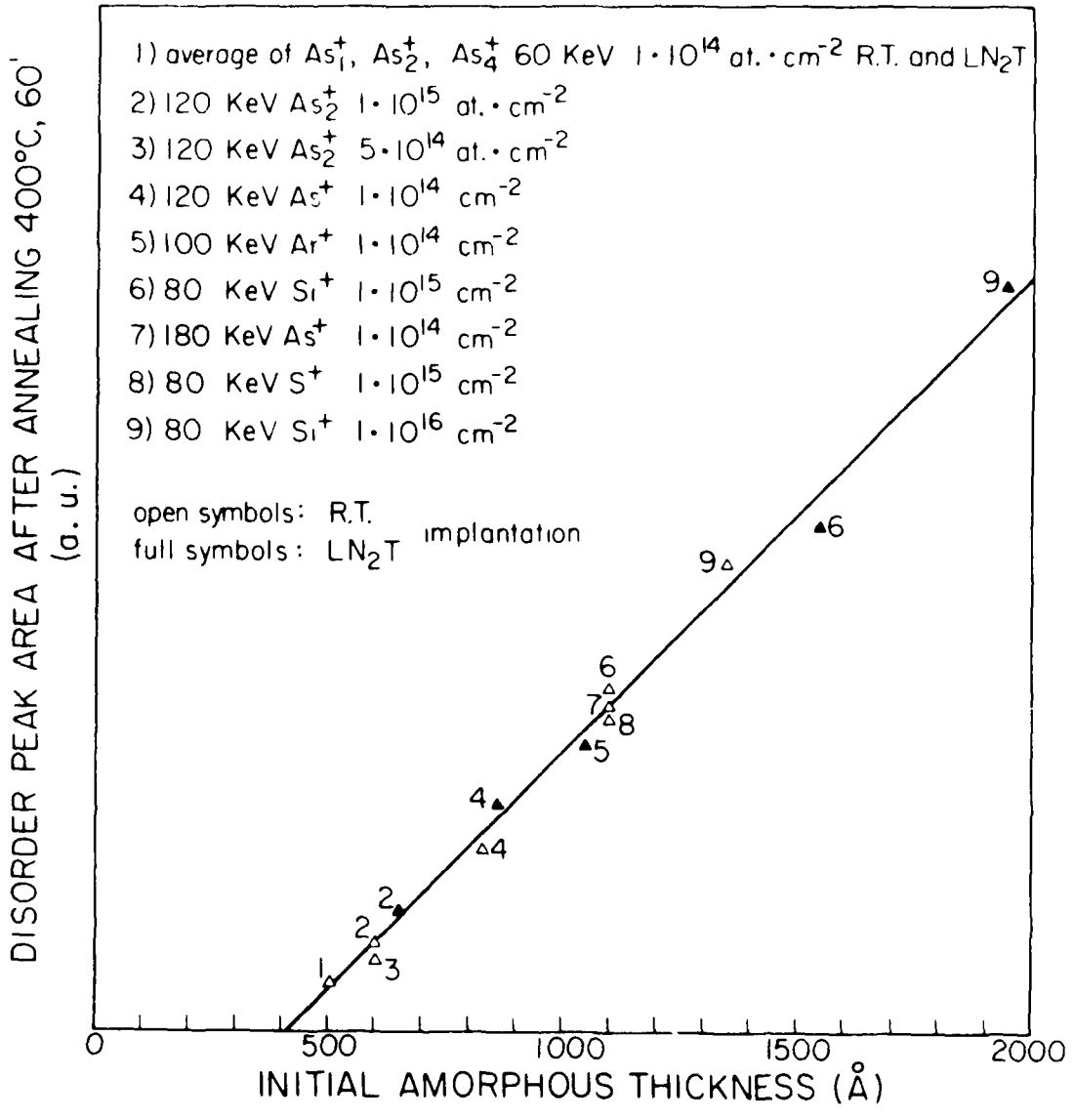

Fig. 3.5-3 Disorder peak are obtained from channeling measurements of implanted GaAs after annealing at 400°C for 60 min as a function of the thickness of the amorphous layer generated by implantation.

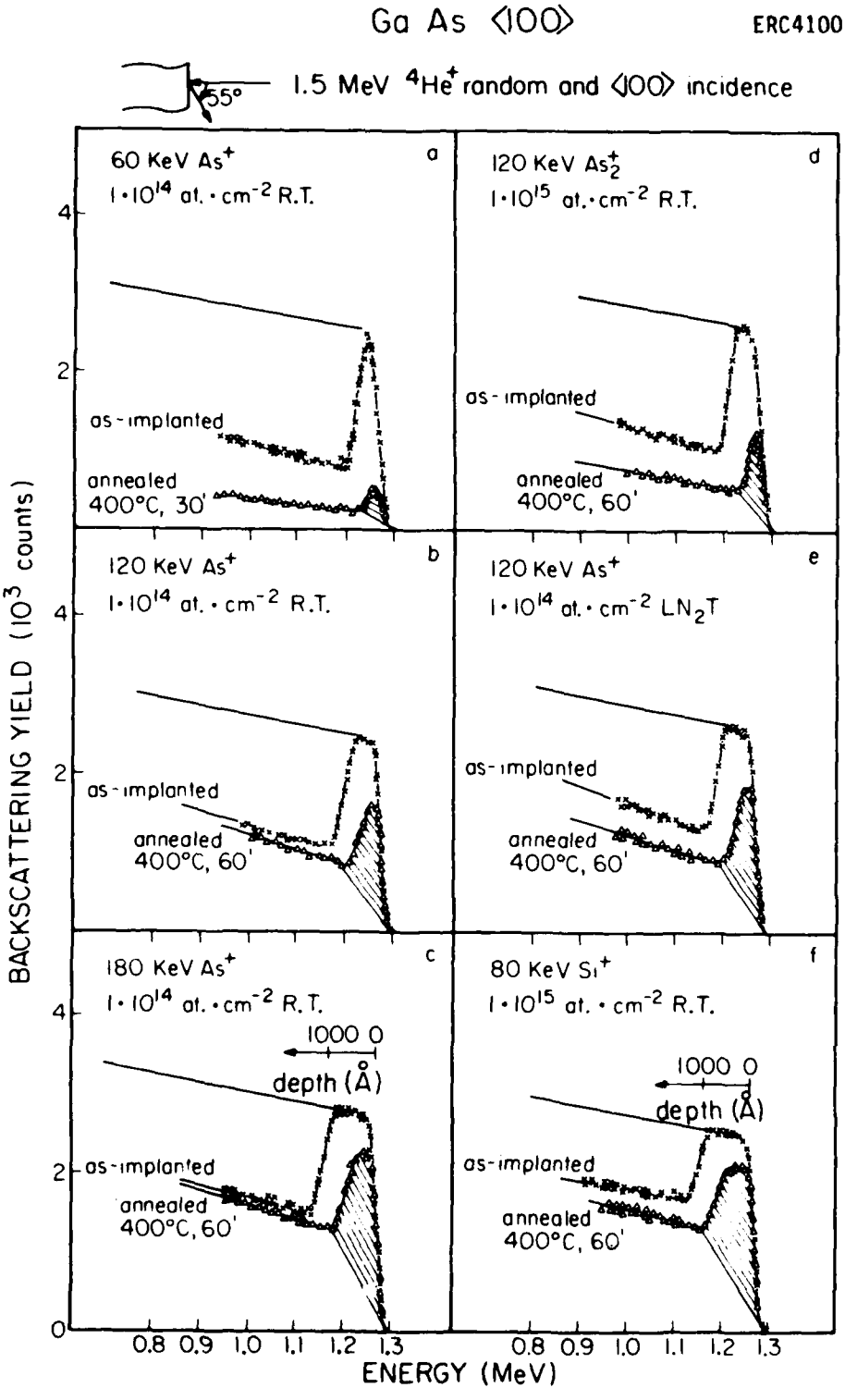

Fig. 3.5-4 Annealing behavior of GaAs implanted under various conditions as labeled. The shaded portions were taken as the disorder peak areas.

reported in Fig. 3.5-3 cannot be explained simply by incomplete regrowth of the thicker layers, but rather reflects an intrinsic property of the regrowth mechanism in GaAs.

The annealing behavior of different amorphous thicknesses is illustrated in detail for a range of different implant conditions in Fig. 3.5-4. Parts a, b, and c of the figure show the disorder profiles before and after annealing for initial amorphous thicknesses of 500, 830, and 1100Å, respectively. The amorphous layers were produced by implanting As^+ ions, all at room temperature and to a dose of 10^{14} ions cm^{-2}, with energies of 60, 120 and 180 keV, respectively. Clearly, the quality of the regrown crystal is best for the thinnest amorphous layer, and it becomes worse with increasing amorphous thickness. Also, it is evident that there is relatively good regrowth for the deepest 400Å of amorphous material and poorer regrowth for the remainder. This is consistent with the extrapolation of Fig. 3.5-3, which indicates "zero" residual disorder for the regrowth of a layer with an amorphous thickness of < 400Å.

Parts d, e, and f of Fig. 3.5-4 show the disorder profiles of samples with the same initial amorphous thicknesses as in parts of a, b, and c, respectively, but produced with different implantations. The sample in d has the same implant specie (As), energy (60 keV) and substrate temperature (room temperature) as the sample in part a, but it has a one order of magnitude larger dose; samples b and e differ in their implantation temperatures; and samples c and f have different species, energies and doses. In each case, not only the areas of the residual disorder peaks are very similar, but the detailed shapes of the backscattering spectra are almost the same.

From the comparison of samples a and d, one concludes that once the GaAs structure is amorphous (as determined from channeling measurements), the introduction of additional radiation damage will not affect the outcome of the regrowth. The argument is particularly convincing in view of the fact that in part d the implantation was performed with As_2^+ ions, where the collision cascade of the two atoms partly overlap, and effects due to excessive amorphization should be enhanced. From the comparison of samples b and e, and c and f one

concludes that neither the amount of self-annealing that may occur during amorphization, nor the amount of energy deposited in the GaAs by an individual impact will alter the outcome of the annealing.

In summary, the results reported in Fig. 3.5-4 indicate first that thermal regrowth as monitored by channeling is independent of how the amorphous state is formed, and second, that the outcome of the regrowth depends primarily on the thickness of the amorphous layer before annealing. The microscopic interpretation of the processes that govern the restructuring of the single-crystal lattice and the way the residual defects evolve during thermal annealing must be derived from microscopic techniques such as TEM and TED.

Figure 3.5-5 illustrates the regrowth behavior of samples in the second state (an amorphous region below a thin non-amorphized layer on the surface). Clearly, there has been good initial regrowth from both sides of the amorphous layer, but there is relatively high residual disorder in the middle, presumably where the two moving crystal/amorphous interfaces met. This type of initial growth occurs only for a narrow range of implantation conditions; the parametric dependence of the regrowth was not studied in any detail. Post-annealing spectra very similar to that in Fig. 3.5-5 have been published previously, but without specific reference to the cause of this form of residual damage.

Regrowth of the samples in the third state (partially disordered crystal) is illustrated in Fig. 3.5-6. The main residual damage here is of a different nature than in the previous cases, primarily causing steps rather than peaks in the channeling spectrum. Such steps are typical of buried bands of defects such as low-angle grain boundaries, dislocations or other defects associated with heavy localized stress. In Fig. 3.5-6 two such bands seem to be present at about 400 and 1000Å depth. Their existence indicates that the initial radiation damage has largely precipitated into clusters localized in depth, or may have migrated to the surface. In all cases, the disorder after annealing is less than that for initially amorphous structures. Also, the lower the implant-induced disorder the lower the residual disorder after annealing. However, it should be noted that these results are in conflict with those of Williams et al.

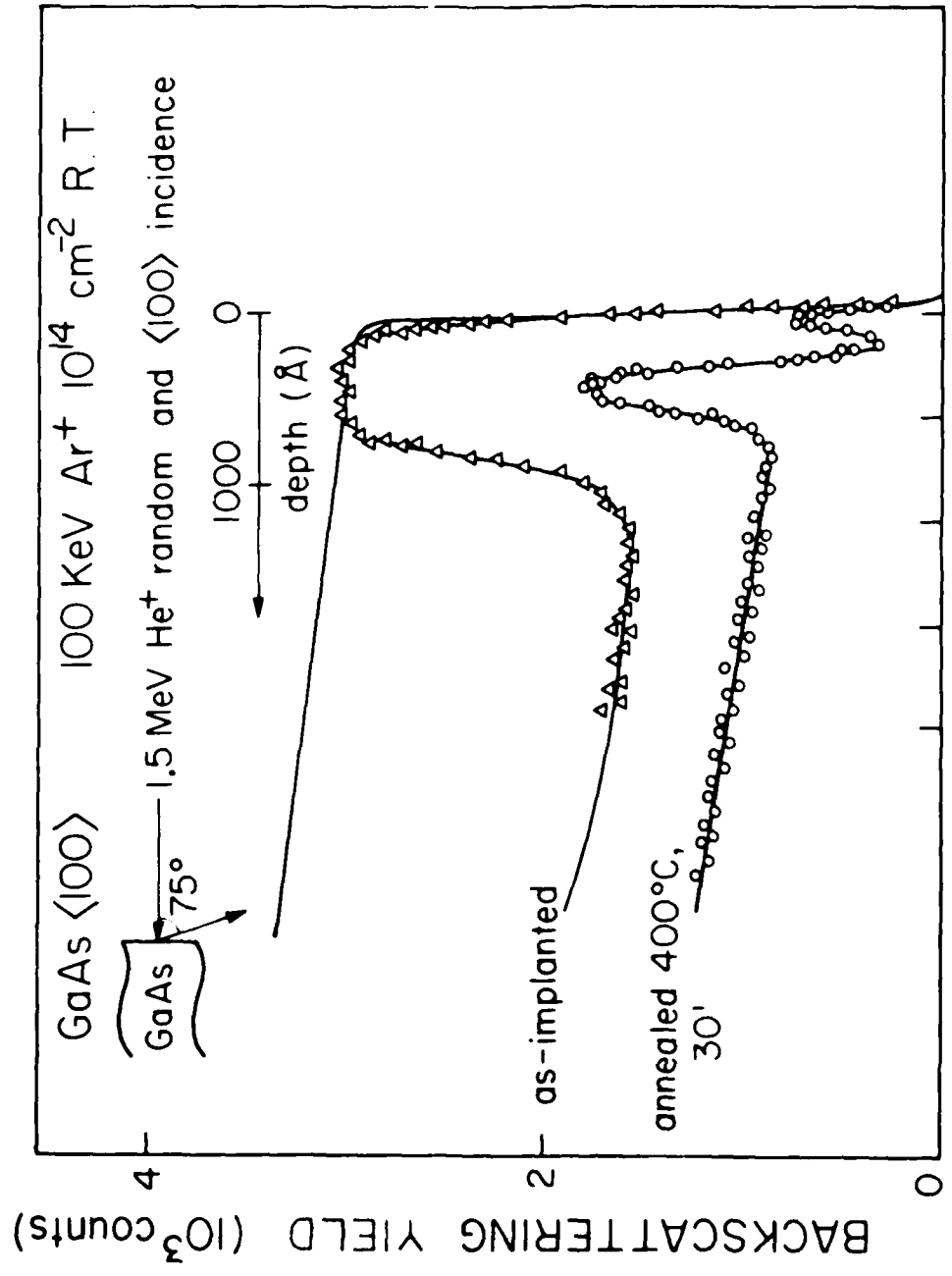

Fig. 3.5-5 Backscattering energy spectra of 1.5 MeV He^+ at random and <100> incidence for GaAs implanted at room temperature with 100 keV Ar^+ to 10^{14} at cm^{-2} and after annealing at 400°C for 30 min.

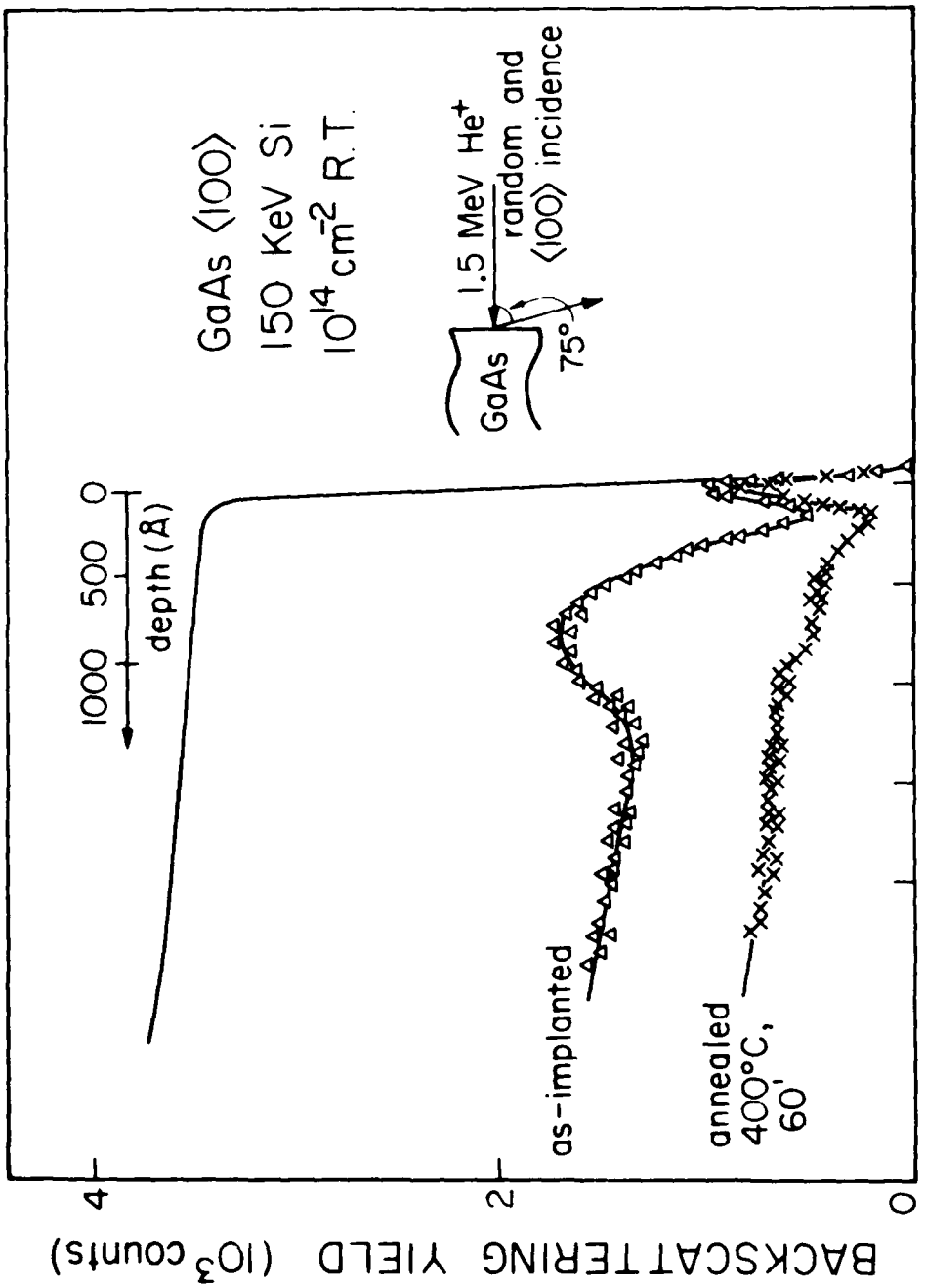

Fig. 3.5-6 Disorder profile for GaAs implanted at room temperature with 10^{14} at cm^{-2} of 150 keV Si$^+$ after implantation and after annealing at 400°C, 60 min.

for implantation of Ar^+ to doses of 10^{14} ions cm^{-2}.[13] Those authors found that the lowest residual disorder was obtained after annealing of the sample with the greatest disorder (a 1300Å layer obtained by implanting at LN_2 temperature). Since the parameters for the implantation of these ions were apparently the same as those used by Williams et al., the cause of the discrepancy is not clear.

4.0 PLANAR GaAs IC PROCESS TECHNOLOGY

The realization of high speed, low power GaAs digital large scale integrated circuits requires a fabrication technology capable of high process yields. The goal of reaching LSI (1000 gate complexity) at the end of this program motivated the choice of a planar fabrication approach to implement the low power Schottky diode FET logic (SDFL) circuit scheme. This fabrication process and circuit concept were formulated and initially investigated under IR&D programs.[15] The full development of the planar implanted GaAs IC the technology has been the focus of the current program.[1]

In the following sections, the status of the planar GaAs fabrication technology used in the demonstration of MSI and LSI circuits is presented and discussed. First, in Section 4.1, the key features of the fabrication approach are reviewed, and the impact of the selected device structure on the development of a very viable as well as versatile process technology is discussed. In Sections 4.2, 4.3. and 4.4, the three main areas of the fabrication technology, localized implantations, circuit lithography and multi-level interconnects, are discussed in detail. This is followed, in Section 4.5, by a review and discussion of wafer processing yields obtained in this program.

4.1 Fabrication Approach and Device Structure

The development of an ion implantation technology in GaAs has made it possible to conceive new fabrication approaches not viable within the limitations imposed by epitaxial layer techniques. This fabrication process capitalizes on the proven uniformity, reproducibility, versatility, and low cost of implanting directly into semi-insulating GaAs for the formation of active device layers.

The observations that the rapid development of Si LSI was greatly facilitated by planar fabrication techniques using ion implantation and dielectric-passivation suggested that similar developments for GaAs would enhance the development of GaAs LSI. This was a guideline in developing this planar GaAs fabrication technology.[16] The drawing of Fig. 4.1-1 represents a schematic

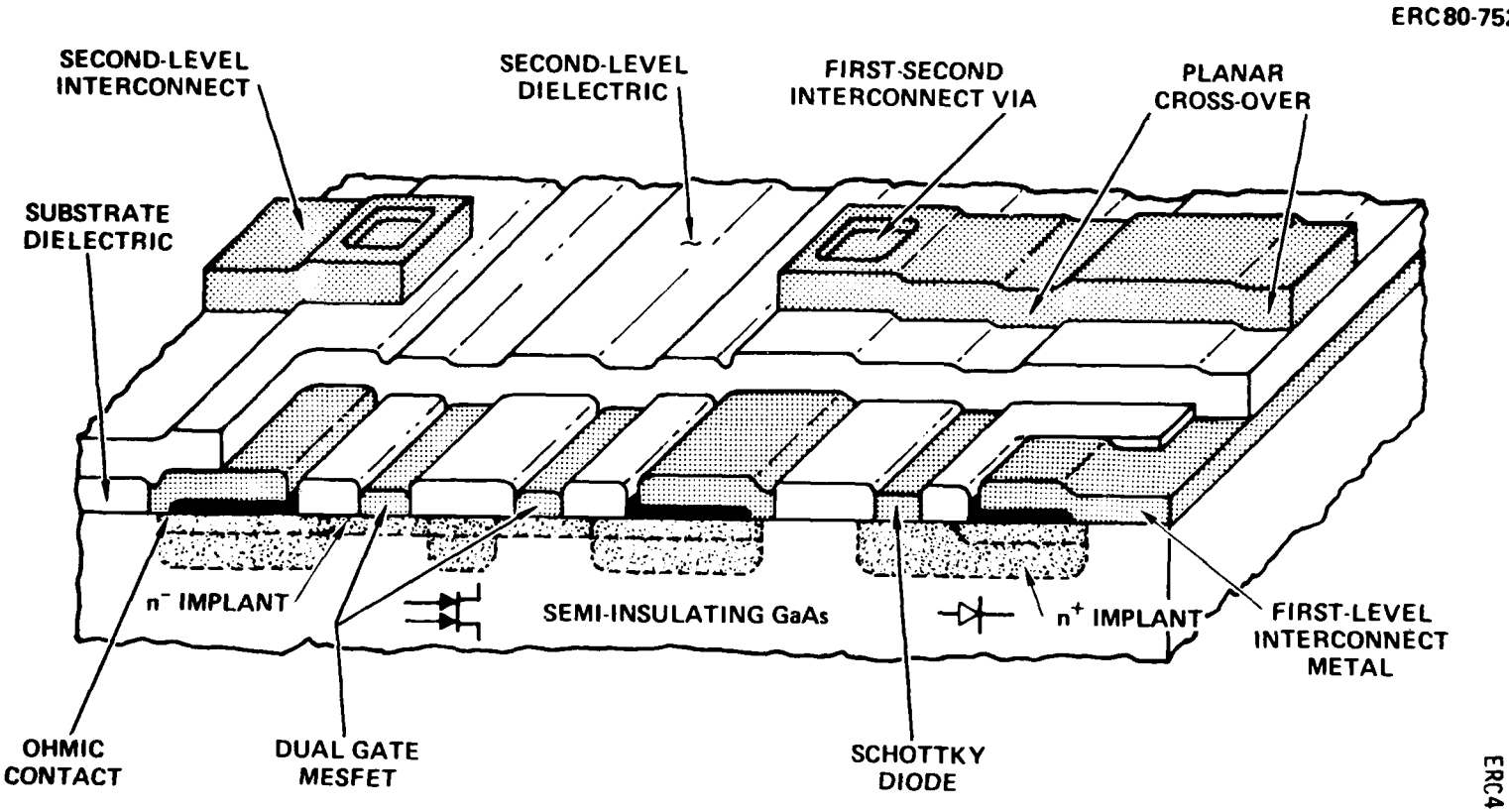

Fig. 4.1-1 Cutaway view of a planar GaAs IC showing a dual gate FET, a diode, and interconnects.

cutaway view of a portion of a planar IC. The planar circuits are fabricated by using multiple localized ion implants directly into semi-insulating GaAs substrates. Hence individual devices can be optimized by using different implants with the unimplanted GaAs substrate providing isolation between adjacent devices. This fabrication method suits the Schottky diode-FET logic (SDFL) circuit approach used in this program since SDFL requires the MESFET and Schottky diodes to have different implanted active layers. The sophistication of this process technology is dramatically illustrated (Fig. 4.1-1) by the use of a 1 μm wide n^+ implant region placed between dual 1 μm MESFET gates in order to lower the channel resistance between the dual gates. Another important aspect of this approach is the use of dielectrics. The dielectric regions shown in Fig. 4.1-1 are utilized for post implantation annealing, protecting the GaAs surfaces during processing, and passivating the surface. Incidentally, this fabrication approach is compatible with any number of implantation steps. Therefore, this process technology has, in principle, the capabilities for producing mixed device types, such as E-MESFET (or E-JFET) and D-MESFET on the same GaAs IC chip.

In Fig. 4.1-2 the Rockwell planar, dielectric passivated, double implanted GaAs MESFET structure is compared to a typical mesa, single implanted MESFET structure.[17] The planar MESFET is fabricated with two implants: one shallow, lightly doped n^- implant forming the channel region, and the other deeper n^+ implant forming the source and drain regions. This design minimizes source and drain series resistance by effectively narrowing the high resistance channel gap between gate and source/drain, and facilitates the fabrication of ohmic contacts. In this manner, excellent device characteristics are obtained without resorting to recessed gate techniques (shown in the lower portion of Fig. 4.1-2). The simplest alternative to this approach is to utilize a single ultra thin, lightly doped layer. However, such a MESFET structure is subject to poor operating characteristics due to the high series resistances resulting from the high sheet resistance (~ 2000Ω/□) of the channel regions between the gate and the source/ drain contacts. The most widely used compromise, which minimizes the effects of high series resistance, consists of using a deeper implant and recessing the Schottky gate into the GaAs surface by chemical etching or

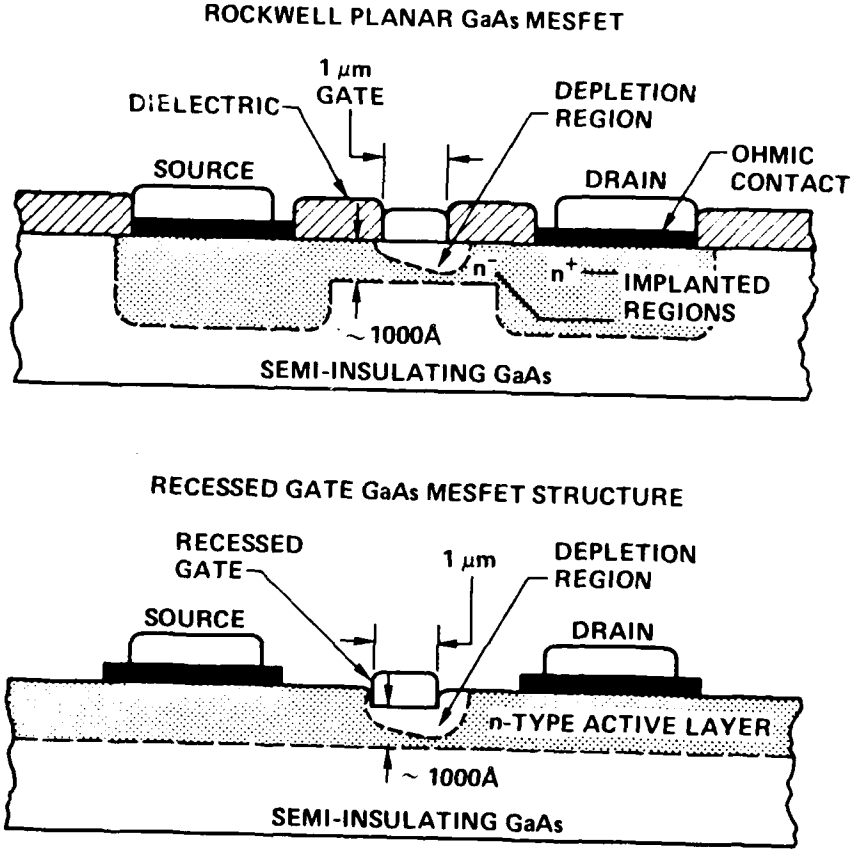

Fig. 4.1-2 Comparison of a planar MESFET fabricated by localized ion implantation with a recessed gate device fabricated on a uniform layer.

anodizaton. This technique provides good FET characteristics, but the uniformity, control and yield of the resulting devices for LSI applications is in serious question. For example, the difficulties encountered in obtaining adequate device uniformity using implanted layers and recessed gate structures for E-MESFET devices has led workers to explore innovative, less demanding circuit concepts (in terms of device uniformity), such as quasi-normally-off MESFET logic.[18]

An important feature of the planar Rockwell approach is the role of the dielectric as an integral element of the device structure. The dielectric, which is used for high temperature post implantation annealing and for protecting the GaAs surface during subsequent processing steps, appears to have a direct effect on device performance. This encapsulation layer above the critical GaAs channel surface region between the gate and source/drain contacts of the FET seems to contribute to maintaining good device characteristics, evidenced by very moderate looping and light sensitivity and by the absence of current "lag" effects.[19] These problems, sometimes observed on non-passivated devices, are possibly associated with exposing bare GaAs surfaces to numerous process steps. Another good feature of the planar MESFETs is the ability of these devices to withstand high electric fields without premature breakdown. Evidence for this claim is presented in Fig. 4.1-3 which shows the I-V characteristics of a planar MESFET operating under high electric field conditions. The device shown is biased from +0.6 V (enhancement) to -1.4 V (depletion) with a 12 V drain voltage much higher than the typical 2.5 V bias. Similar devices have operated to 20 V without failure. These data show that MESFETs fabricated with this planar process are very rugged and do not fail easily under adverse conditions (e.g., voltage transients). This reliable performance (no premature breakdown) is attributed to the heavier doped implanted region under the ohmic contacts, the use of ion implanted layers (no epitaxial/substrate interfaces) and the channel surface protection provided by the dielectric between the gate and the source/drain electrodes. Although the ruggedness of the devices is not directly capitalized on in low power digital logic applications, it may contribute positively to device reliability.

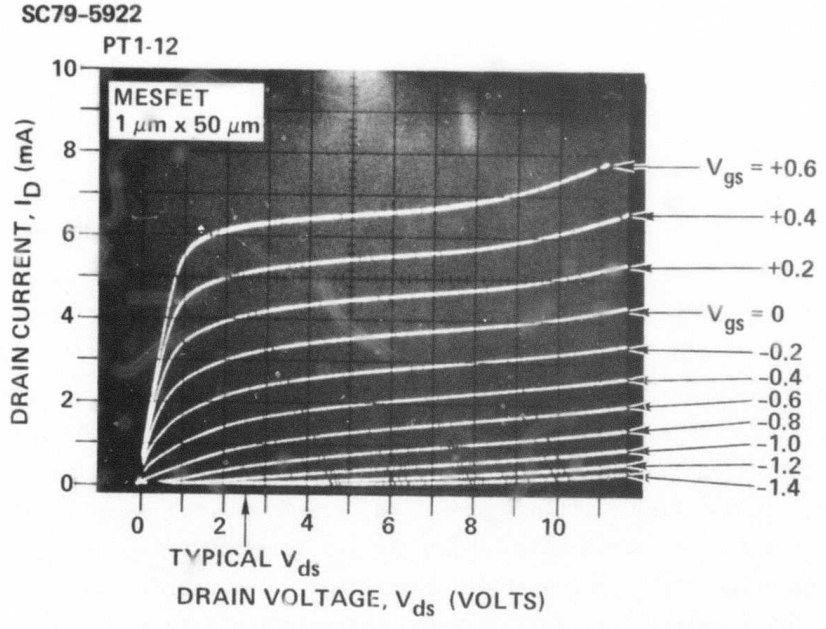

Fig. 4.1-3 I-V characteristics of a planar MESFET showing the excellent high field behavior of the device. Note that typical operating V_{ds} does not exceed 2.5 V.

Another performance factor which is very important to digital IC logic is presented in Fig. 4.1-4. These data, taken on a planar MESFET, show a sharp current response to gate voltage pulses at a repetition rate of 10 kHz. Similar behavior is observed over a wide range of repetition rates from 50 Hz to 50 kHz. There is no current "lag" (delay) in these planar MESFET devices. Current "lag" effects have been attributed to GaAs surface states in the region between the gate and the drain.[19] As suggested earlier, the stable, high quality dielectric which remains in the critical MESFET channel surface region protecting and stabilizing the surface is believed to be responsible for this good device behavior.

Summary of Planar GaAs Process Steps

The planar GaAs IC fabrication process utilizes many state-of-the-art processing techniques. A summary of the key processes and methods used is shown in Table 4.1-1. Since GaAs ICs are designed with 1 μm features, a dry process has been developed. The only wet chemical process steps are associated with the photolithography and photoresist lift-off technique. A brief summary of the current fabrication process steps (shown schematically in Fig. 4.1-5) is also presented here in order to serve as a guide for the more extensive process discussions which follow. This process sequence has proved very workable at the MSI/LSI level. The original process scheme remains virtually unchanged since no major problems which would cause significant alterations have been identified. However, this process technology must be regarded as still under development. Further adjustments to the process will take place as necessary in the future.

SC79-5892

PLANAR MESFET

W = 50 μm

G_L = 1 μm

V_P = -1.2V

PULSE REPETITION RATE

10 KHz

BIAS VOLTAGE

V_{dd} = 2.5V

LOAD RESISTANCE

10Ω

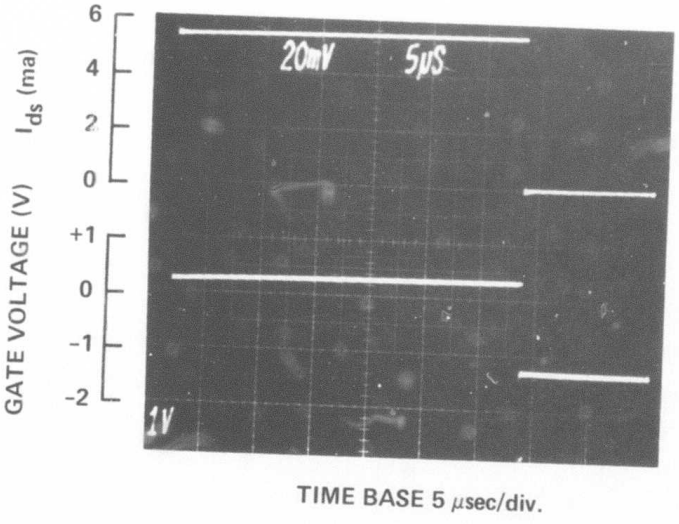

Fig. 4.1-4 Transient response of an SDFL gate.

Table 4.1-1

Summary of the GaAs planar IC fabrication steps (see Fig. 4.1-5).

A) Material Preparation and Dielectric Deposition - Step (1)

Cleave wafer (25 mm x 25 mm)
Clean wafer for backside Si_3N_4
Backside Si_3N_4 (RF sputter)
Wafer preparation, polish, and etch (Br-Methanol)
Frontside Si_3N_4 (RF sputter)

B) Multiple Localized Implants - Steps (2-5)

First implant (n^-) photomask (Canon 4X)
n^- Se implant
Implant registration etch (RIE)
Implant photoresist mask removal (O_2 Ash)
Second implant (n^+) photomask (Canon 4X)
n^+ S implant
Implant registration etch (RIE)
Implant photoresist mask removal (O_2 Ash)
SiO_2 encapsulation (RF sputter)
Anneal

Plasma Etching Notations:
Reactive Ion Etch - (RIE)
Plasma Etch - (PE)
Plasma Etch with Oxygen - (O_2-Ash)

C) Circuit Lithography - Steps (6-8)

Ohmic contact photomask (Canon 4X)
Ohmic contact window etch (RIE/PE)
Ohmic contact meltalization (AuGe/Pt)
Ohmic contact definition (dielectric assist lift-off)
Alloy ohmic contacts (450°C)
Schottky 1st level metal photomask (Canon 4X)
Schottky 1st level window etch (RIE/PE)
Schottky gate metalization (Ti/Pt/Au)
Schottky metal definition (dielectric assist lift-off)
dc wafer-probe (Pretest/Mapping)

D) Multi-Level Interconnects - Steps (9-11)

Wafer Cleaning (O_2-Ash)
Second level dielectric (plasma Si_3N_4)
Via window photomask (Canon 4X)
Etch via windows (RIE)
Second level metalization (Ti/Au)
Second level interconnect photomask (Canon 4X)
Second level metal etch (ion milling)

E) Final Encapsulation (Optional for Packaging)

Wafer cleaning (O_2-Ash)
Third level dielectric (plasma nitride)
Bonding pad and kerf line photomask (Canon 4X)
Etch bonding pads and kerf lines (RIE)

Plasma Etching Notations:
Reactive Ion Etch - (RIE)
Plasma Etch - (PE)
Plasma Etch with Oxygen - (O_2-Ash)

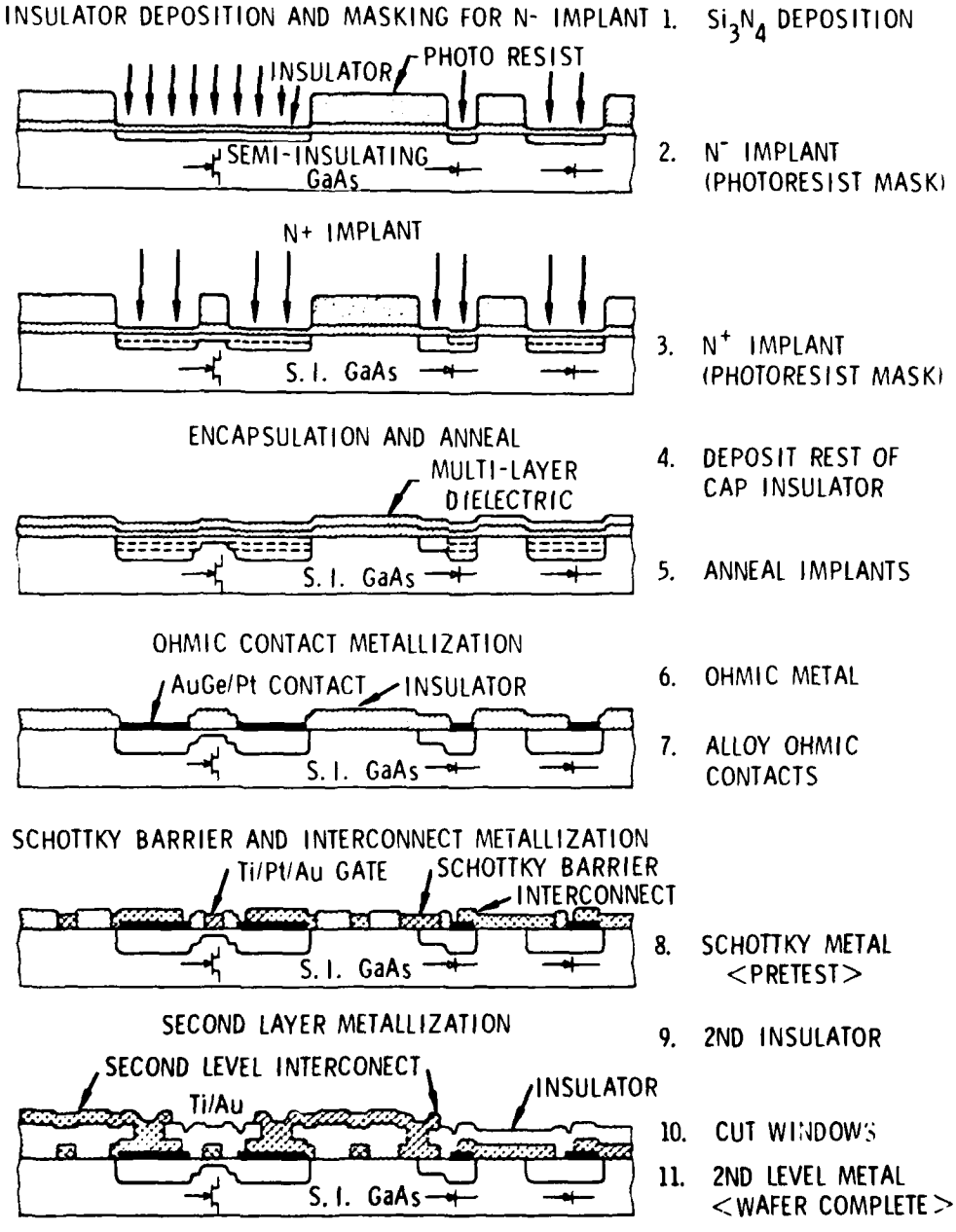

Fig. 4.1-5 Planar GaAs IC fabrication steps.

4.2 Localized Ion Implantation

Ion implantation is now an established material technology for GaAs ICs and for many discrete GaAs devices as well. Many workers, however, still appear to be using mesa, single implanted fabrication processes. Since mesa structures are only easily implemented with a single implantation step, this approach inherently restricts device and cicuit optimizaiton. In the current program, the power of ion implantation was fully exploited by developing a multiple localized implant technology ideally suited to SDFL logic, which requires optimization of individual device (MESFET and Schottky diode) active layers.

The implant process steps used in the fabrication process were shown in Fig. 4.1-5 (Sec. 4.1). Initially, the semi-insulating GaAs substrate is coated with a thin layer of Si_3N_4 which remains on the wafer throughout all the subsequent processing steps. The first process steps are the two localized implantations carried out through the thin Si_3N_4 layer using thick (~ 1.5 μm) photoresist as the ion beam mask. After each implant, a shallow step is plasma etched into the Si_3N_4 for registration of the implanted regions. Following the implants, additional dielectric (SiO_2) is added prior to the post implantation annealing step. The same dielectric used in annealing also provides an intermediate layer lift-off medium used in the processing of first level metal interconnects (see Section 4.3).

Normally, a sequence of two implants is used in this planar IC process; however, this process is capable of any number of implantation steps that may be necessary in order to optimize individual devices. An example would be an additional high dose (n^{++}) implantation step to heavily enhance the doping under ohmic contacts. Investigations into using additional n^{++} implants for ohmic contact device optimization had been planned. However, they were not carried out because very low specific ohmic contact resistance ($<10^{-6}$ Ω-cm^2) was reached without this third implant. This additional implant remains an option if future process developments will require it.

Typical implantation parameters and the resulting electron concentration profiles for both IC implants conducted through the Si_3N_4 cap are shown in

Fig. 4.2-1. The 400 keV Se implantation profile is peaked near the GaAs surface due to the energy absorbed in penetrating the thin Si_3N_4 layer. Little influence, except for the shift of the peak of the implanted profile, has been observed as a result of implanting through thin dielectric layers. The theoretical predictions of enhanced doping from "knock-ons" (see Sec. 3.3) from the Si_3N_4 cap during ion implantation has not been identified in these implanted profiles, nor has any shift been observed in the peak of the Se profile as a result of small variations in dielectric thickness. The low dose implants ($<10^{13}$ cm^{-2}) used in this work do not appear to significantly damage the dielectric since there has been no evidence of any change in the dielectric etch rate after implantation. However, it is possible that applications requiring much higher implant doses (i.e. n^{++} contacts) will be subject to problems associated with "knock-ons" and/or resulting damage to the encapsulating dielectric. For example, high dose implants ($> 10^{14}$ cm^{-2}) into SiO_2 are known to enhance its etch rate. High dose, through the cap implants, are yet to be fully explored and will be the subject of further investigations.

Referring to Fig. 4.1-5 and 4.2-1 the S implant provides a conductive layer much deeper (~4000Å) than the FET channel implant (n^-). This S implanted layer (called n^+ to differentiate it from the n^- layer) is ideally suited for the high speed switching diode required in SDFL. Both n^- and n^+ implants are used for level shifting diodes and for enhancing the doping under ohmic contact regions. The S profile is deeper and the resulting electron carrier concentration much lower (~ 30% activation) than the predicted LSS calculated profile for this energy and dose. These differences can be attributed to a cap dependent enhanced diffusion mechanism.[20] Low S activation and the relatively flat implant profile are due to sulfur atoms outdiffusing to the GaAs/Si_3N_4 interface. Extensive S outdiffusion appears to be unique to a highly stressed cap such as Si_3N_4.

In order to routinely monitor the sheet resistivity of the implanted active layers, test cells are provided on the PM chip of the IC masks (Section 5.1). A survey of sheet resistance for the individual implantations and for a combination of both implants measured on a number of processed GaAs IC wafers yielded the average sheet resistivities values shown in Table 4.2-1.

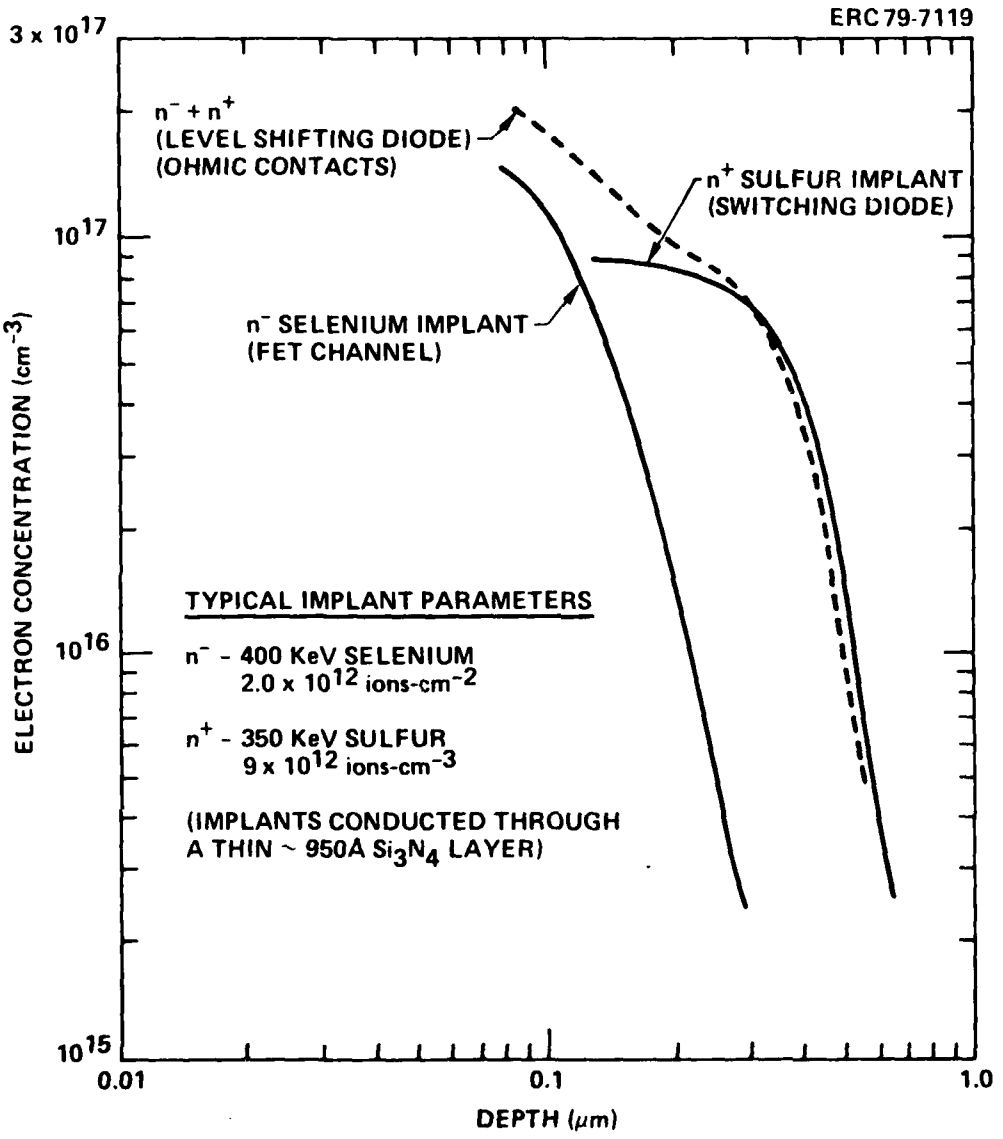

Fig. 4.2-1 Active layer profiles (for the n^- FET channel Selenium implant and the n^+ high-speed switching diode sulfur implant.

Table 4.2-1

Multiple Implanted Planar GaAs IC Sheet Resistivity of Selenium and Sulfur Implants

Implant	Region	Device	Sheet Resistivity $\bar{\rho}_s$ (Ω/□)
Selenium	n^-	FET	2503
Sulfur	n^+	Switching Diode	495
Se + S	$n^- + n^+$	Level Shifting Diode Ohmic Contacts	392

As is suggested from the implant profiles and sheet resistance values, the most difficult layer to control is the shallow lightly doped high resistance n^- MESFET channel layer. This implant step is critical since this layer directly controls the MESFET pinchoff voltages. The n^+ implanted layer used for the high speed switching diodes has a somewhat more relaxed specification since the main concern for this device is that it must be fabricated on a relatively high conductance-low carrier density layer for low series resistance and low capacitance of the diode.

Reproducibility and Uniformity Control for the n^- Layer

GaAs IC process control of reproducibility and uniformity depends both on the quality of the semi-insulating GaAs material used and the characteristics of the planar GaAs fabrication processes. Both factors must be considered to be of equal importance. Here, the degree of reproducibility reached by the planar fabrication process is discussed, and factors particularly important in controlling reproducibility are identified.

A good perspective for this discussion can be obtained by first examining the GaAs ion implanted profiles in Fig. 4.2-2. These data were taken before the start of the present GaAs IC process development program.[21] The figure shows several low dose Se profiles obtained by implantation into wafers from five different semi-insulating GaAs ingots. The implants were made into bare GaAs substrates which were subsequently encapsulated with the same reactively

Energy = 400 keV

Dose = $1.8 \times 10^{12}/cm^2$

Implant T = 350^0C

Anneal 850^0 - 30 min

Boule No's.
1903
2000
2004
2100
2440

$N_{max} = 8.2 \cdot 0.8 \times 10^{16} cm^{-3}$

X at 70% of N_{max} = 2100 ± 100Å

X at 10% of N_{max} = 3125 ± 245Å

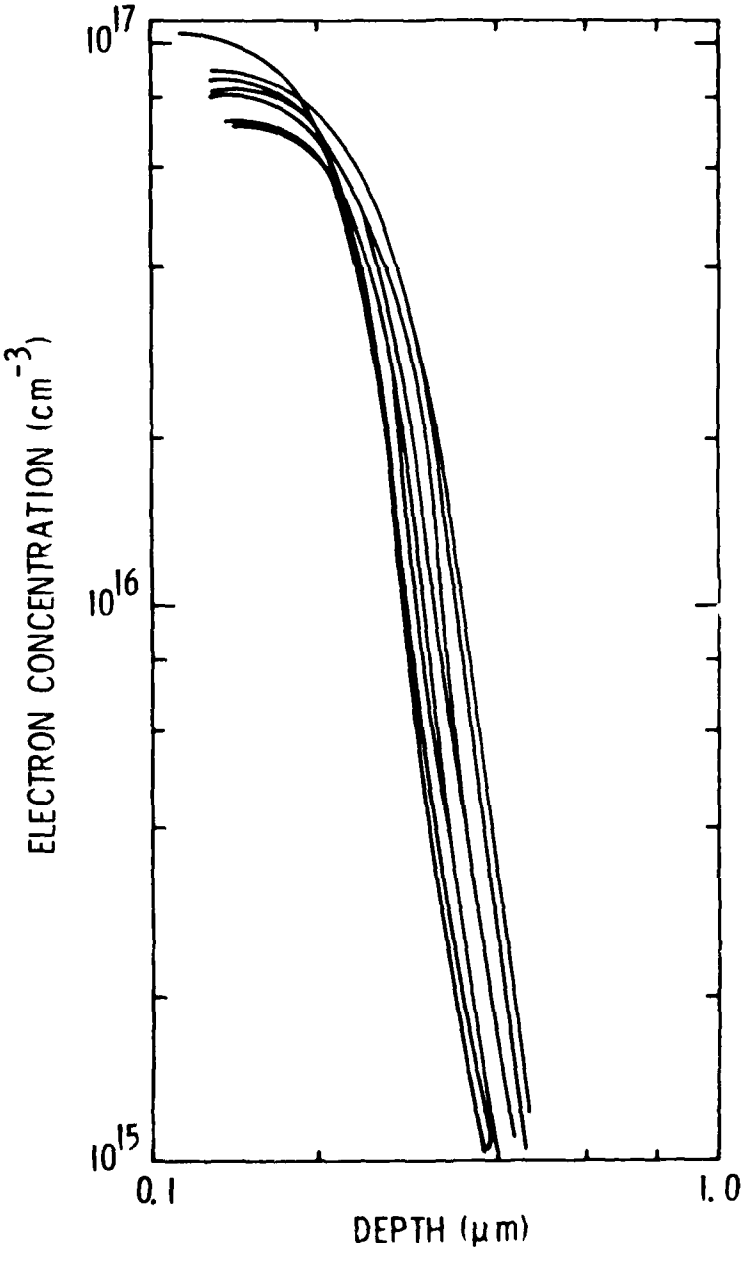

Fig. 4.2-2 Active layer profiles obtained by implantation of Se into wafers from 5 different ingots. These data, obtained before the beginning of this program, represent the state-of-the-art in 1977 (reprint from Ref. 3).

sputtered silicon nitride cap and annealed. At the time when these data were obtained they represented the state-of-the-art for reproducibility of Se implantation into GaAs. A key figure of merit for comparison is the depth, x, at 10% of N_{max} equal to 3125Å, with a standard deviation of 245Å.

Data from a survey of implantations performed over the past two years are shown in Fig. 4.2-3. These profiles were obtained by implanting through a thin Si_3N_4 layer, thus yielding shallower (~ 2200Å) profiles than the bare implants shown in Fig. 4.2-2. The statistical base is much larger involving 11 different ingots, ~ 60 test chips altogether, and 21 different Si_3N_4 caps. The spread of profiles is smaller as evidenced by the standard deviation of 173Å, as compared to the previous 245Å standard deviation shown in Fig. 4.2-2. The fact that the recent survey covers a very large period of time (2 years) adds significance to the degree of reproducibility attained. The spread in profile depth in Fig. 4.2-3 can be translated into a spread of voltages required to deplete these layers to the 10^{16} carrier concentration level. Such voltages are encompassed between 1 and 1.6 V, with a standard deviation of 0.33 V. The reproducibility of doping profiles shown in Fig. 4.2-3 represents an improvement over what was possible two and half years ago, and it is quite acceptable for SDFL circuit applications at the present level of integration.

From analysis of reproducibility data it has become clear that the variations of doping profiles arise to a large extent from subtle differences between semi-insulating GaAs substrates. It has been observed that profile reproducibility is better when the implant profiles are compared on wafers from a single ingot. Figure 4.2-4 shows a group of low dose Se implanted profiles measured on 16 different slices from the same GaAs ingot. The standard deviation of the voltages required to deplete the layers to 10^{16} cm^{-3} is only 0.11 V (as opposed to the 0.33 V for 11 ingots in Fig. 4.2-3). The standard deviation of profile depth (measured at 10^{16} cm^{-3}) is 64Å (as opposed to 173Å for 11 ingots in Fig. 4.2-3). The variation of MESFET pinchoff voltages from wafer to wafer would be expected to be of the same magnitude as the depletion voltages measured on the C-V profiles.

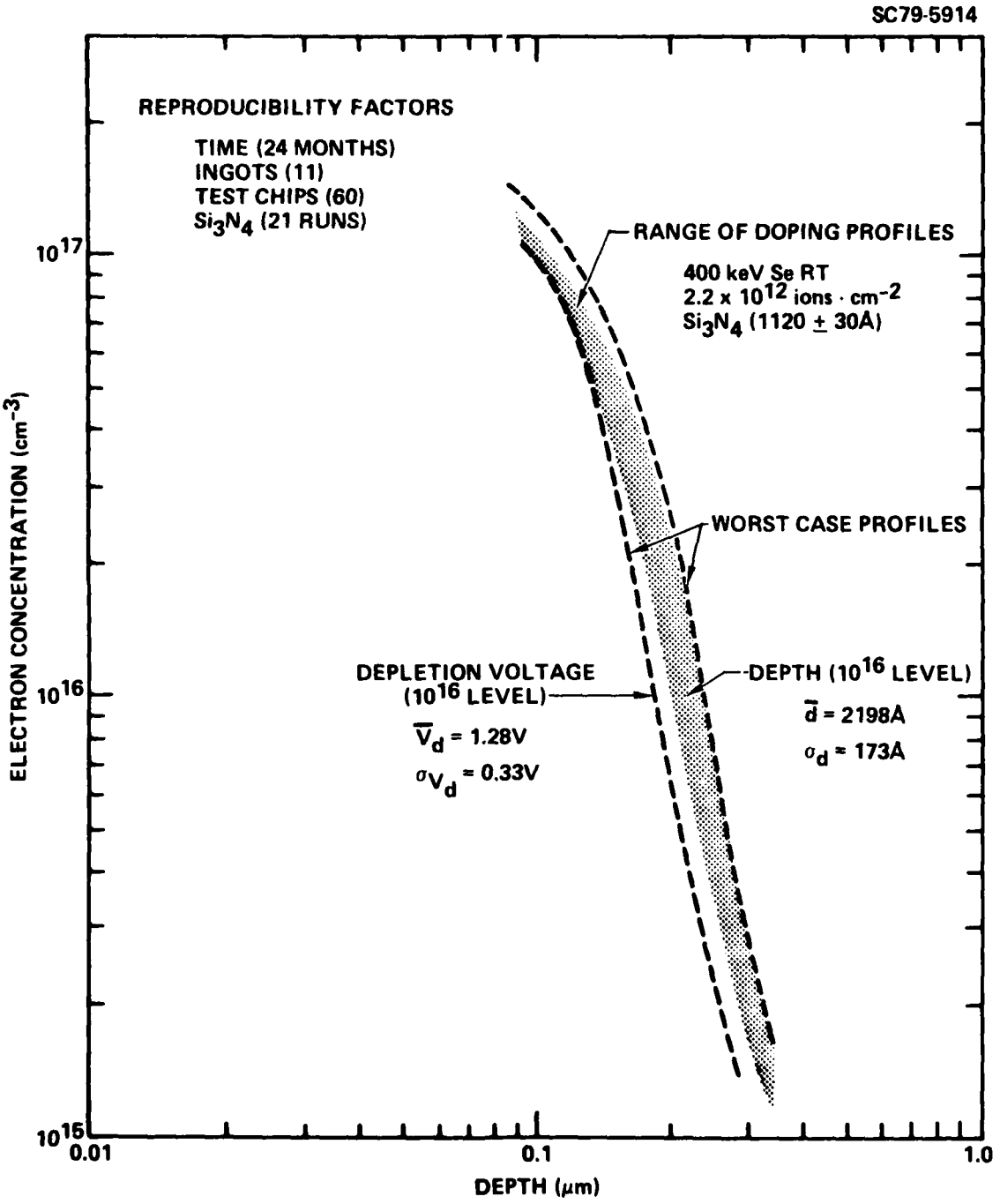

Fig. 4.2-3 Summary of doping profiles obtained by Se implantation through a thin cap into semi-insulating GaAs over a long period of time (2 years).

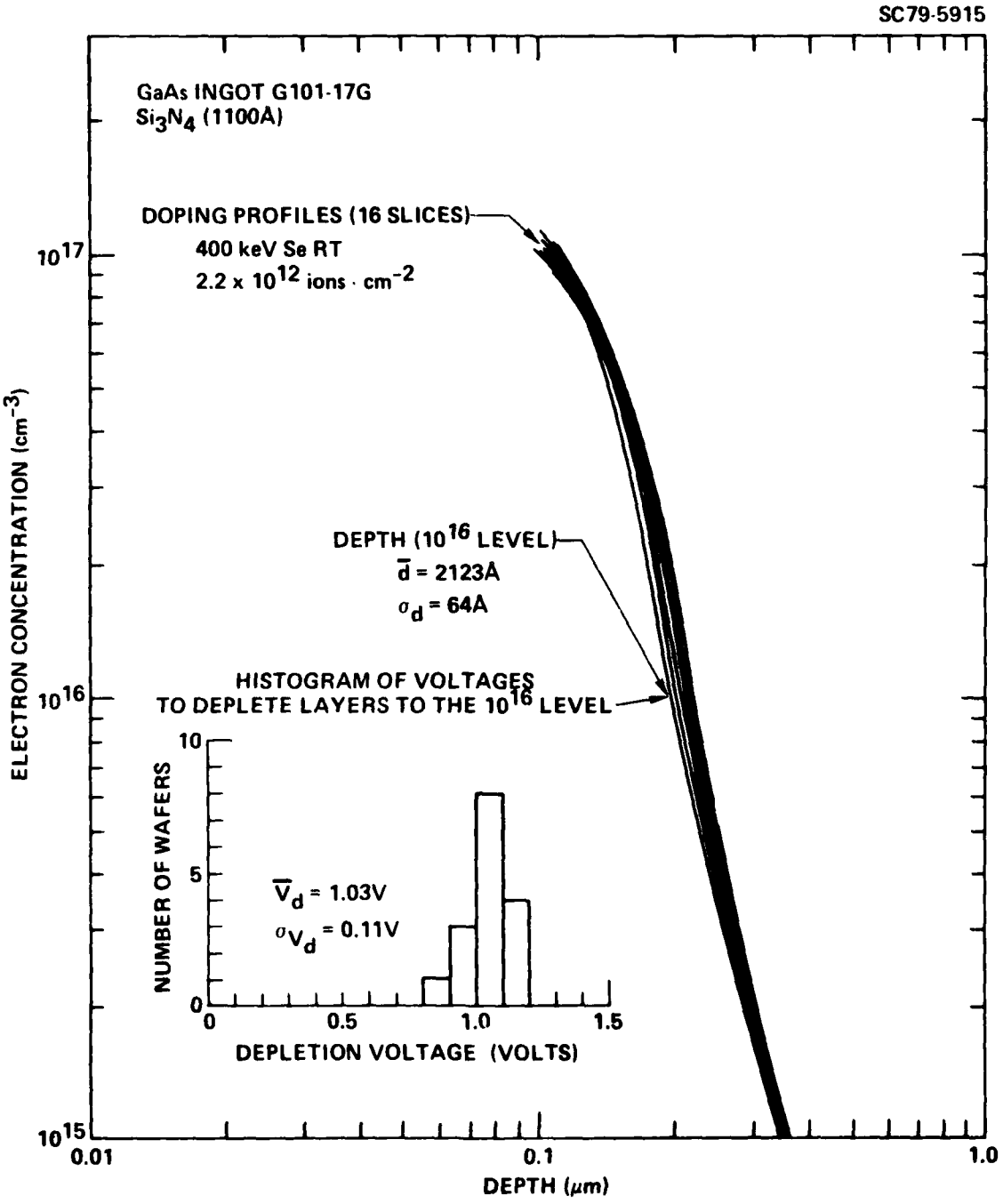

Fig. 4.2-4 Doping profiles obtained by Se implantation through a thin cap into semi-insulating GaAs substrates, all from the same ingot.

Having concluded that a single IC qualified GaAs ingot results in good doping profile reproducibility, it is possible to perform implantation dose adjustments to accommodate small variations between different ingots. The data shown in Fig. 4.2-5 were taken from 72 planar GaAs, 1 μm long gate, MESFETs (50 μm wide) regularly distributed over the wafers (in the T2 test areas described in Sec. 5.2). In order to get similar device characteristics, different implantation doses were required for each ingot. In this case, a dose of 2.3×10^{12} cm^{-2} for ingot XS3757 provided the same MESFET pinchoff voltages as the 2.0×10^{12} cm^{-2} dose used on ingot G101-22G. As can be seen, all the pinchoff voltages were within a 1 - 1.2 V range with standard deviations between 8% and 11% of the average values (91 to 121 mV). Test profiles measured as part of the IC material qualification procedures provide the information used to tailor the implantation dose for individual ingots. In this manner good reproducibility is achieved between various IC process lots using different GaAs material. Although this is a manageable approach at the current level of GaAs IC development, future large scale manufacturing efforts will require more consistency in the GaAs material. Efforts already under way at Rockwell (Section 3.1.2) and at Crystal Specialities (Section 2.1) are aimed at specifically addressing this issue. A practical near term improvement anticipated, will be the availability of much larger ingots, hopefully providing a large number of wafers (~ 100 or more) from the same ingot for processing.

Another critical requirement for LSI is uniformity of device characterisics. As indicated from these discussions, the most difficult layer to control and the key to device performance is the shallow lightly doped high resistance n^- MESFET channel layer. This active layer directly controls the pinchoff voltage V_p and is the key parameter in the optimization of the logic gate speed and power dissipation. However, control of this critical parameter goes well beyond the quality of semi-insulating GaAs substrates. The reproducibilty and uniformity of the planar processes used are at least as critical as the quality of the material. In the early development stages of the localized implantation process there was concern that the sophisticated process techniques necesary for planar SDFL (as opposed to simple mesa, single implant methods) would lead to inferior

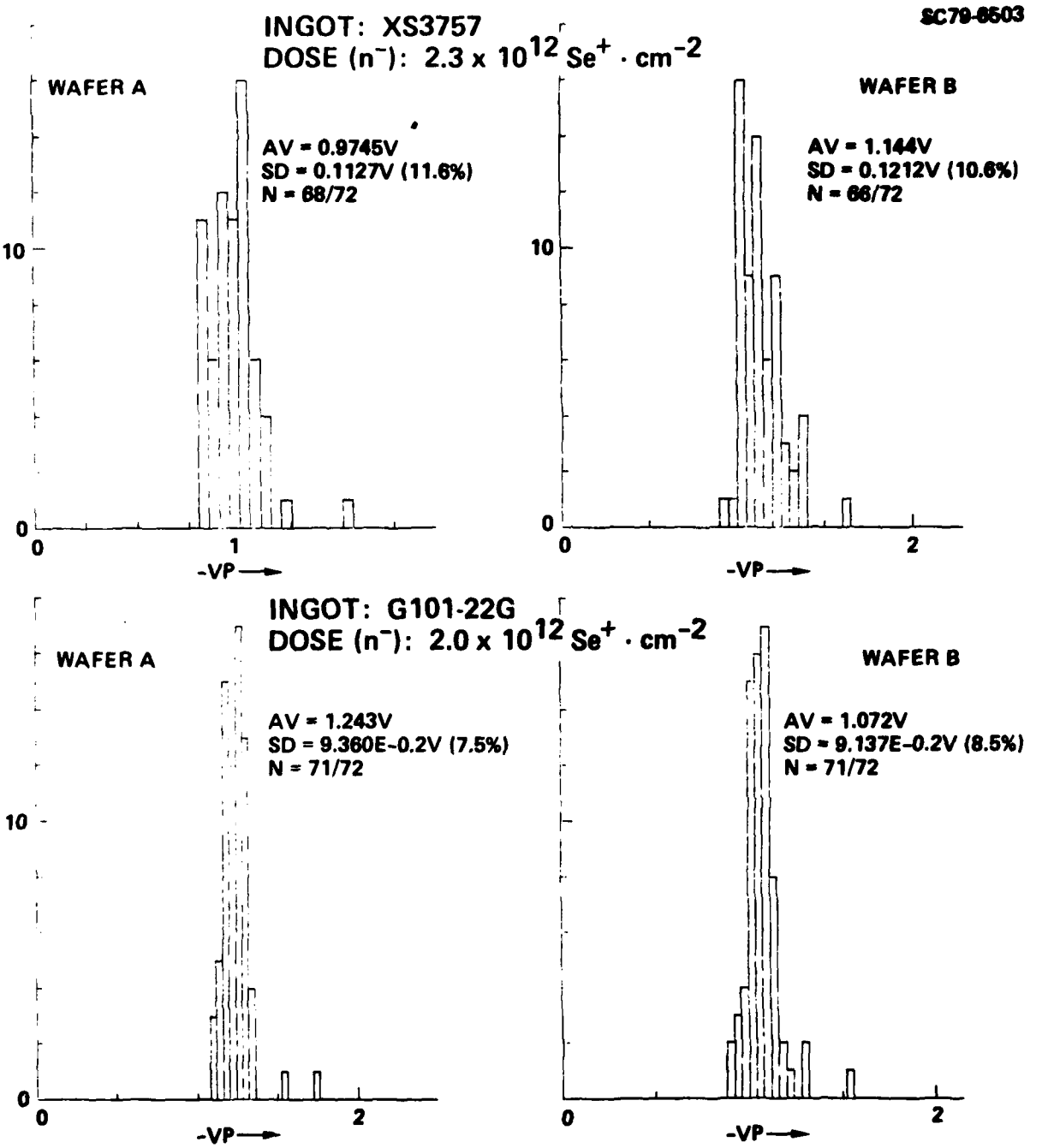

Fig. 4.2-5 Histogram of pinchoff voltage for 72 test FETs (1 μm gate length, 50 μm channel width) for 4 wafers processed from two semi-insulating GaAs ingotsd. These data show the reproducibility of device characteristics.

process results. Instead, excellent results have been achieved showing the outstanding superiority of the localized implant approach.

Excellent active layer uniformity and control of this planar process is evidenced by the histograms of typical V_p distributions of planar, double implanted dielectric passivated MESFETs, shown in Fig. 4.2-6.[22] The long range V_p distribution of 71 FETs from a full GaAs IC wafer are character zed by a V_p of 1.24 V with a standard deviation of 94 mV. The area encompassed by these distributed V_p measurements would accommodate over 10^5 GaAs SDFL gates. Short range statistics of 81 FETs distributed over an equivalent 50 gate area show an outstanding 37 mV standard deviation. It should be emphasized that these are average data, not the best achieved (see Sec. 5.4). This excellent device uniformity reflects the present state of GaAs material, ion implantation and fabrication process capability.

In summary, it has been shown that the best reproducibility of doping profiles is achieved by using wafers from the same GaAs ingot, and that the uniformity of device characteristics over a wafer is good. Overall process reproducibility is achieved by monitoring the small profile variations between different semi-insulating GaAs ingots, and by adjusting the implantation dose accordingly. The material and localized implant techniques are capable of supporting large scale integration.

Silicon Implants

As already discussed in Sec. 3.2, Si implants are being investigated as a possible addition (n^{++}), or replacement for some or all of the implantation species. Silicon appears to be the only ion species that could serve as a "universal" n-type implant ion in GaAs. The insert table and profiles shown in Fig. 4.2-7 illustrate how Si implanted profiles can satisfy both the MESFET and Schottky switching diode requirements.

As can be seen in Fig. 4.2-7, the appropriate choice of Si implant energy and dose results is a profile which resembles very closely the standard IC Se profile used for the FET channel. However, merely replacing the current

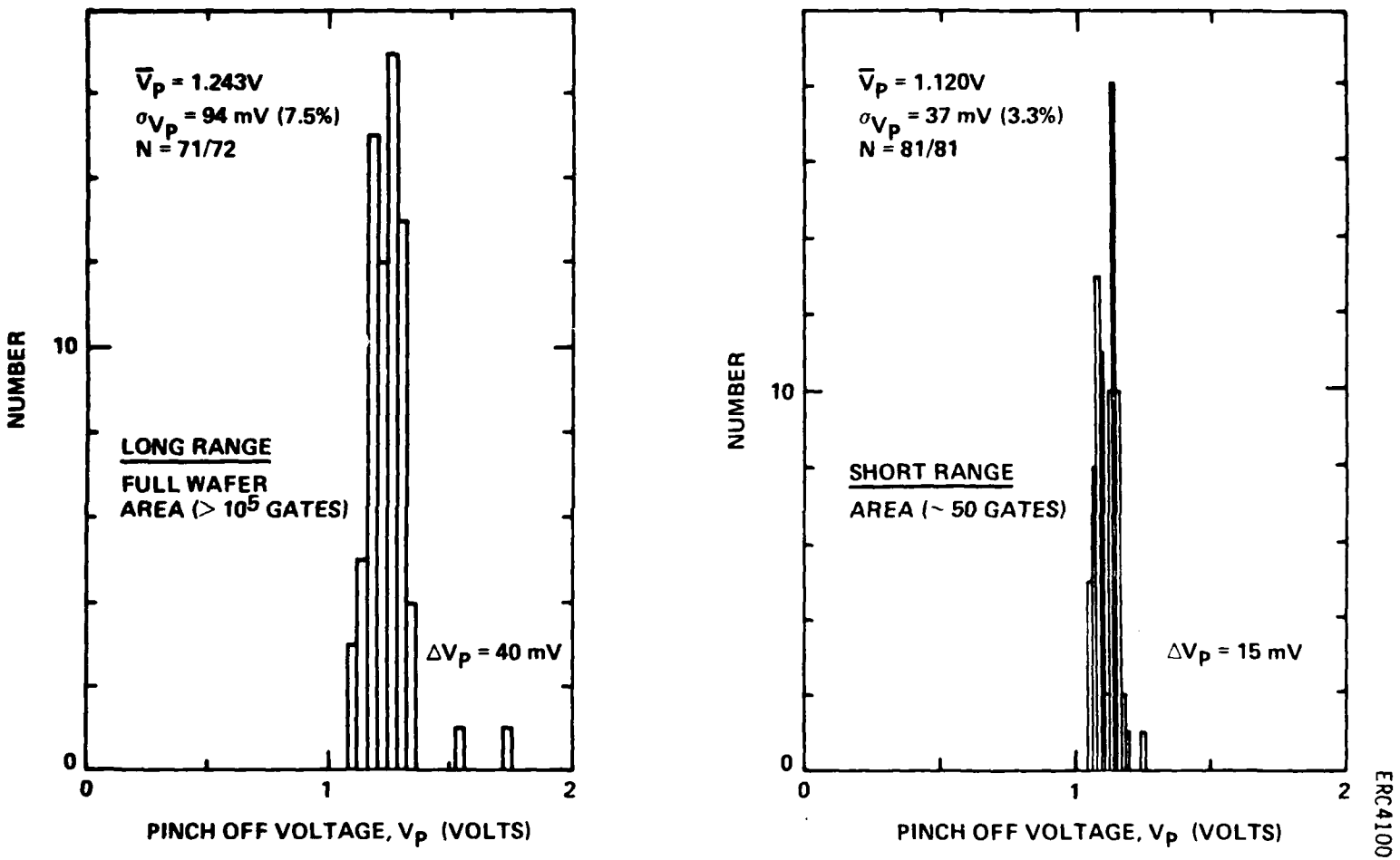

Fig. 4.2-6 Histogram of pinchoff voltages of test FETs comparing the uniformity for an array coarsly spaced over a wafer and a dense array (circuit size).

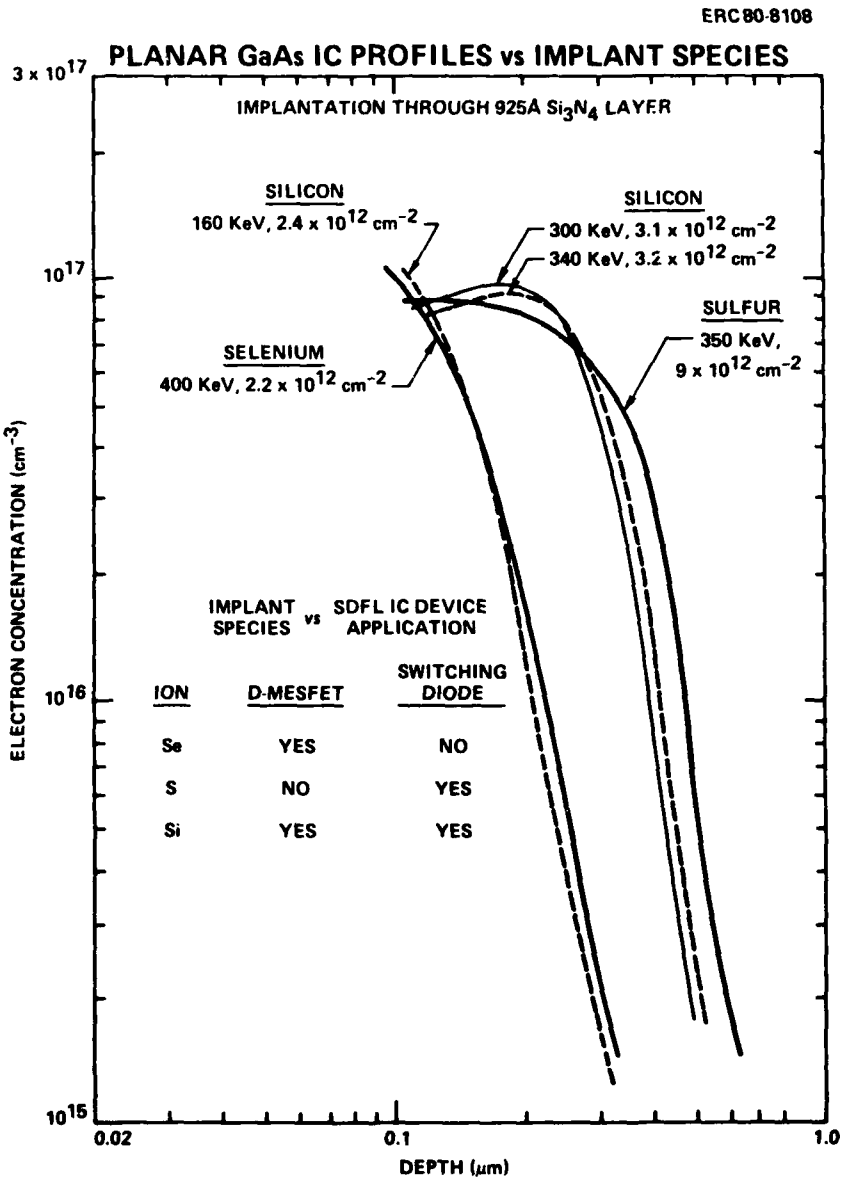

Fig. 4.2-7 Carrier concentration profiles for Se, Si, and S implants.

Se and S profiles with Si implanted profiles is not sufficient. In the case of MESFET channel profiles, reproducibility is a key issue for further work. It is possible that the lower mass of Si may result in less implantation damage than that caused by Se for room temperature implants (room temperature implants are desired in the process); there is also the probability of fewer Si and N "knock-ons," also due to the lower mass. Thus Si may provide more reproducible n-type profiles. Si profile reproducibility and uniformity investigations need to be carried out to fully determine the potential of Si implantations.

There is further motivation for Si implants replacing S implants in both Schottky barrier diode and ohmic contact applications. For Schottky barrier diodes, Si profiles appear to be better suited to matching the "ideal" profile. As shown in Fig. 4.2-7, the Si profiles are peaked at a depth of ~ 2000Å with some fall off towards the GaAs surface. This profile conforms to the requirements for high speed Schottky barrier diodes, namely high conductance (deep, high carrier concentration) and low capacitance (low carrier concentration in the surface region). Another benefit of Si over S is that it is likely to be more reproducible. The deep Si profiles shown in Fig. 4.2-7 appear to exhibit ~ 90% activation as opposed to ~ 30% activations for S. This is evident when Si (3.1 - 3.2 x 10^{12}-cm^{-2}) and S (9 x 10^{12}-cm^{-2}) doses resulting in roughly equivalent profiles are compared. Since sulfur implants experience low activation, there would appear to be a higher probability for non-reproducible results. Experiments planned for comparing Si implants with S implants will be carried out to yield conclusive results on this subject.

In the ohmic contact implant application, the out diffusion characteristics of sulfur also manifests itself in lateral diffusion. It is believed that this contributes to the differences observed between vertically and horizontally oriented MESFETs (see Sec. 3.4). Silicon should exhibit less diffusion and, possibly, less orientation sensitivity of the FET characteristics.

Experiments have begun utilizing Si implants for the n^+ implantation step. Figure 4.2-8 shows MESFET and Schottky barrier switching diode I-V characteristics comparing Si vs S implanted devices. The device characteristics

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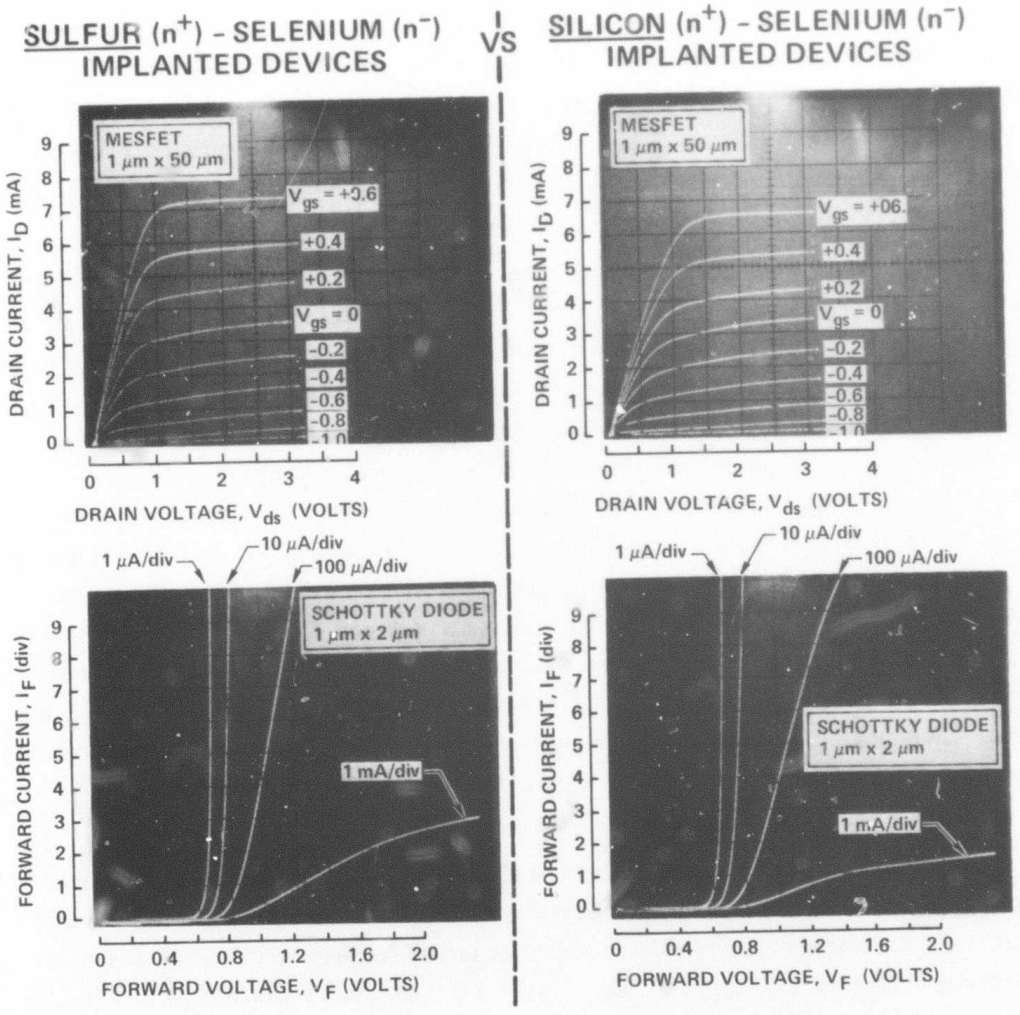

Fig. 4.2-8 Planar GaAs MESFET and Schottky barrier diode I-V characteristics comparing Si implants vs S implant.

are quite similar. However, in this experiment, the Si implant parameters (250 KeV, 3.5 x 10^{12}-cm^{-2}) resulted in higher than optimum sheet carrier concentrations characterized by a lower saturation current level in the Si implanted diode and a slightly higher saturation voltage in the Si implanted MESFET. Additional work is in progress to evaluate Si implants for Schottky barrier applications.

4.3 First Level Circuit Lithography

The planar GaAs IC fabrication process shown in steps 6-8 of Fig. 4.1-5 (Sec. 4.1) is the focus of this discussion. While acknowledging the importance of the localized implant processes (Sec. 4.2) it is the first level circuit lithography process that encompasses the most crucial steps in the fabrication of planar GaAs ICs. Since GaAs ICs by necessity are designed with 1 μm features, a dry LSI compatible process capable of high yield has been under development.[1,22]

The same basic fabrication steps are followed in the fabrication of the ohmic contacts and the first layer metallization which includes Schottky barriers, gates, and first-level interconnects. The ohmic contacts for the FETs, active loads, and Schottky diodes use an AuGe/Pt metallization system, whereas the Schottky barriers, gates, and first-level interconnects use a Ti/Au or Ti/Pt/Au system. Before this step in the process the entire surface of the GaAs wafer is covered with dielectric. The metallizations are fabricated by defining the desired patterns in photoresist, and plasma etching the underlying Si_3N_4/SiO_2 dielectric to the GaAs surface. The desired metal layer is then evaporated, and the circuits are defined using a photoresist lift-off technique (see Fig. 4.1-5, steps 6-8). This technique results in the metallizations being self-aligned precisely within the dielectric windows.

This unique lithography process has consistently produced, 2 μm x 2 μm ohmic contacts, 1 μm x 2 μm Schottky barriers, 1 μm long gates, and first-level interconnects down to 1.5 μm with good yield. In the following, details of the important elements of these processes will be discussed, including reduction

photolithography, dielectric assisted lift-off techniques, and details on the ohmic contact and Schottky metal processes.

Reduction Photolithography Process

Common to all of the GaAs IC process steps is the delineation of fine line resist patterns required for the fabrication of these circuits. Over the reporting period fabrication of GaAs ICs has been accomplished at ERC by using a Canon 4X projection mask aligner. The Si industry, due to recent emphasis on VLSI, is also gradually adopting this photolithography technique in the form of direct step on wafer (DSW) systems. Reduction projection photolithography has several advantages: there is no mask wear as in contact printing; any mask step-and-repeat error or small defect on the mask is reduced by a factor of 4 at the wafer level; and alignments are precise, typically within 0.5 μm. An example of the 1 μm resolution capability of this photolithography technique is shown in the scanning electron micrograph of Fig. 4.3-1. In principle, as shown in this edge view of dual 1 μm gate openings, relatively vertical photoresist side walls and excellent alignment can result from this photolithographic technique.

Although Fig. 4.3-1 demonstrates that excellent photoresist patterns can be obtained, practical process considerations dictate that variations in photoresist resolution and edge acuity across wafers must be anticipated. This is highly dependent on wafer flatness, photoresist thickness variation, and local circuit topography.

Historically, replication of 1 μm geometries on GaAs has been accomplished by using direct photoresist lift-off methods. When direct photoresist lifting is used for defining metal patterns, excellent edge acuity of the photoresist profile is absolutely necessary. However, in practice such good edge acuity is difficult to attain with reproducibility through reduction projection photolithography (or any other photolithography method) at the 1 μm resolution level. This is due to the small depth of focus (±1.5 μm) required in this photolithography technique which makes the sharpness of the exposure very sensitive to wafer flatness currently specified to ±1.5 μm (see Sec. 3.1).

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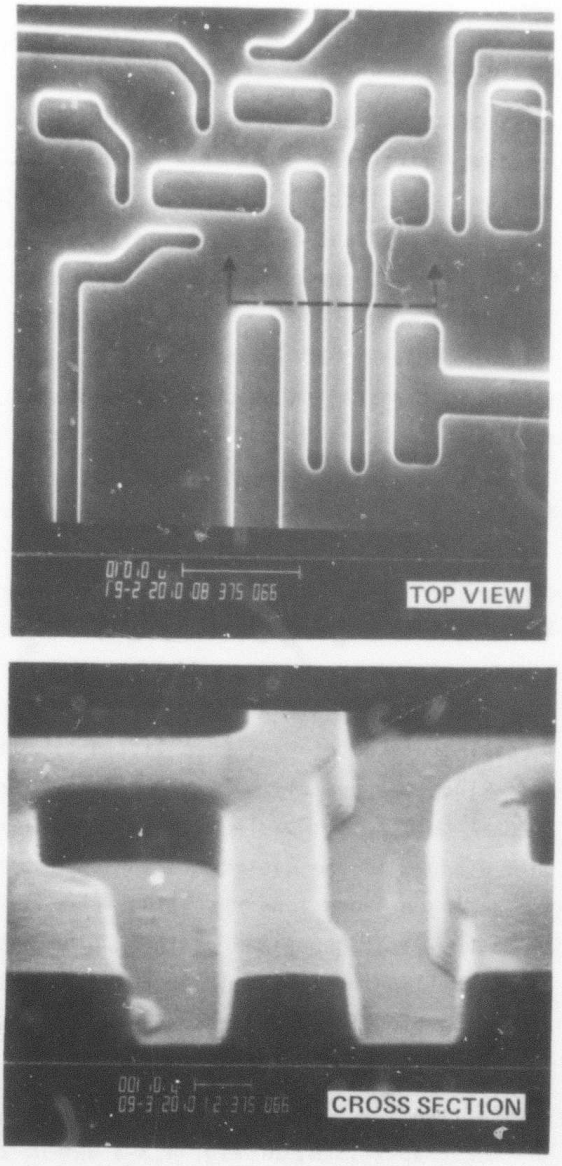

Fig. 4.3-1 SEM photograph highlighting dual 1 μ gate photoresist patterns defined by projection photolithography.

Therefore, in order to ensure high process yields, enhanced lift-off techniques have been developed.[22]

Dielectric Assisted Lift-Off Process

The process described here makes use of the dielectric covering the wafer as an intermediate lift-off medium (see Fig. 4.1-5). A schematic of the resulting intermediate layer lift-off technique is shown in Fig. 4.3-2 (left side) compared with a conventional direct lift-off process (right side). The intermediate lift-off technique using dielectric is easy to implement and very reproducible. It eliminates two fundamental limitations of direct lift-off, the need to use thin metal films (<5000Å), and the need to use strong resist solvents and harsh mechanical agitation which can lead to marginal process yields. The resulting metal profile using direct lift-off technique is usually very coarse as illustrated in the right side of Fig. 4.3-2. The explanation for this coarse, low yield structure is as follows: during the metal evaporation process, metal deposited on the GaAs substrate also fills up the side wall of the photoresist and in most cases (without special undercut photoresist profile techniques) becomes connected to the metal deposited on the photoresist top surface (seen in Fig. 4.3-2 right side). Hence, there is need for thin metal films and strong agitation during the lift-off process. In contrast, the intermediate lift-off process (called dielectric assisted lift-off) does not suffer from these limitations. Since the underlying dielectric is plasma etched, the deposited metal (metal thickness < dielectric thickness) lies below the photoresist layer within windows in the dielectric and is actually slightly shadowed by the photoresist during evaporation, resulting in deposited metal films which are not connected to the metal deposited on the top of the photoresist. (See the discussion on via filling presented in Sec. 4.4 and SEM cross sections illustrating these principles.) The unwanted metal is easily lifted away by simply dissolving the photoresist in acetone.

The merits of the intermediate lift-off technique can be judged in the scanning electron micrographs (SEM) of Fig. 4.3-3 where, on the right side, a

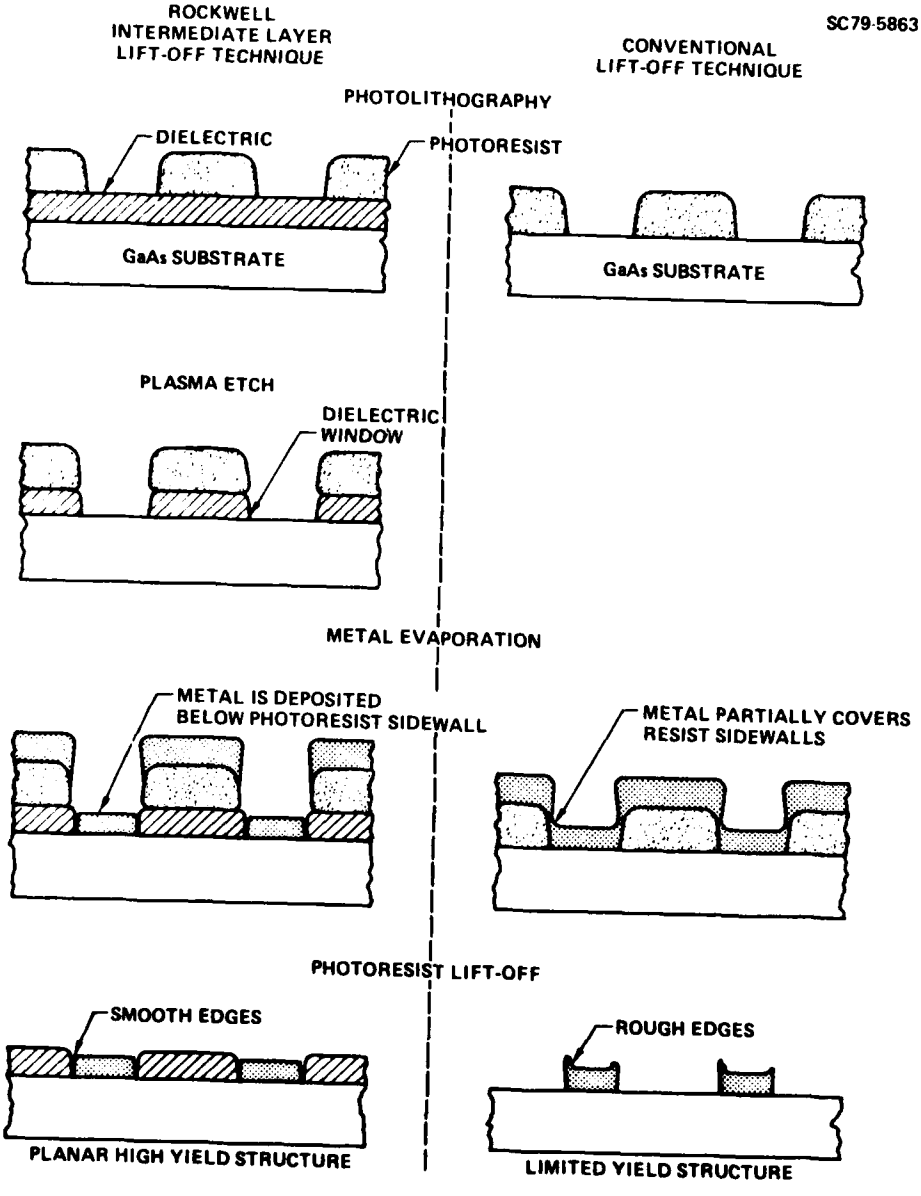

Fig. 4.3-2 Comparison of lift-off techniques.

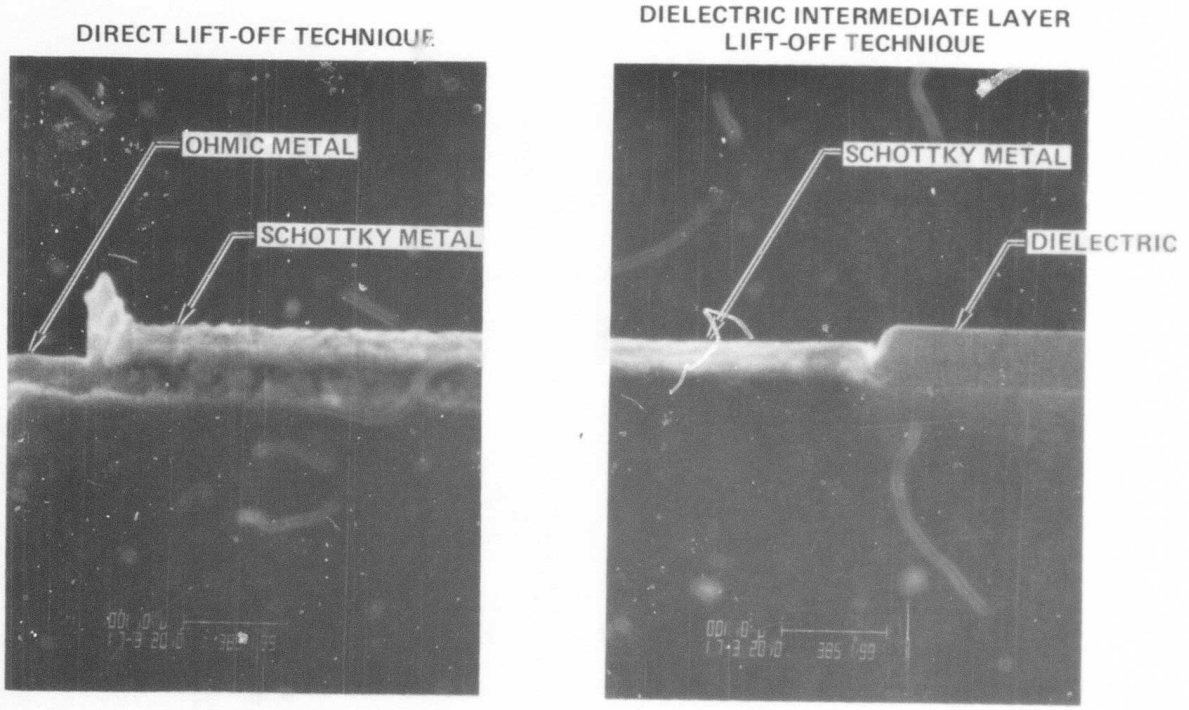

Fig. 4.3-3 Comparison of the results of direct lift-off and intermediate layer lift-off techniques.

smooth Schottky metal structure is precisely aligned within the dielectric opening. The smoothness of this structure can be compared with the example of direct lift-off shown on the left portion of Fig. 4.3-3. This SEM photograph shows the region where Schottky metal is used as an overlay over ohmic contact metal and illustrates the coarse metal edge often resulting from using direct lift-off techniques.

While additional refinements are necessary, the dielectric assisted lift-off technique has demonstrated high yields with the added advantage that metal contacts and interconnects are automatically precisely registered within dielectric windows. The sophistication of this lithographic technique for fabricating planar, high yield, dense 1 μm structures precisely aligned within dielectric windows is highlighted in Fig. 4.3-4. This scanning electron micrograph of a portion of a planar GaAs IC shows an SDFL gate containing a dual 1 μm gate MESFET. The ability to fabricate such dual gate SDFL circuits has provided GaAs ICs with new multi-level logic approaches for optimizing increasingly complex circuits.[23] Also, recent IR&D supported work has demonstrated that this process, when used in conjunction with E-beam lithography, is fully compatible with fabricating 0.5 μm long gates.

Another important benefit from this process approach stems from the planar structure. As shown in Fig. 4.3-5, fabricating the first-level metal within windows in the first-level dielectric and maintaining the first-level metalization thickness close to the dielectric thickness results in a planar structure which greatly facilitates the fabrication of complex multilayer interconnects.

The upper portion of Fig. 4.3-5 shows the smooth crossovers resulting from this planar multi-layer fabrication approach. The planar crossovers eliminate any potential problems such as shorts between first and second level interconnects, and high resistances or open interconnects resulting from poor step coverage. The lower portion of Fig. 4.3-5 illustrates how these interconnect difficulties can easily exist when poorly defined first level metal is used in conjunction with conventional multi-level crossover techniques. A full discussion on the multi-level interconnect process follows in Section 4.4.

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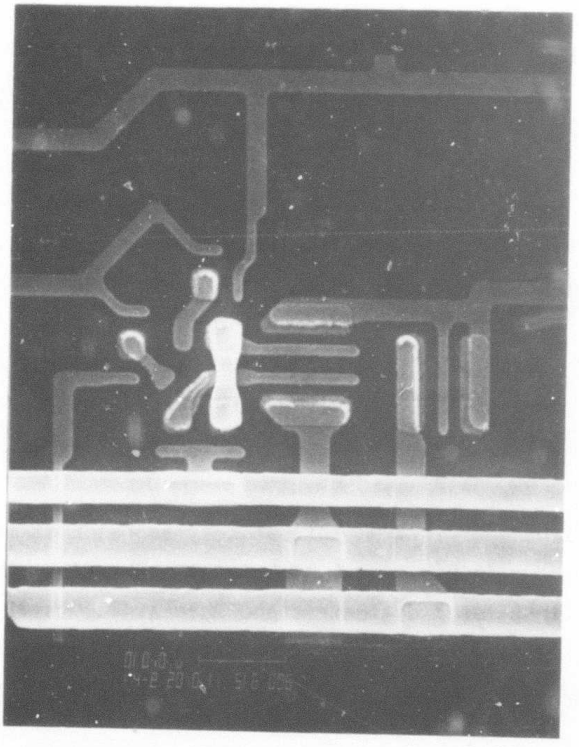

Fig. 4.3-4 SEM photograph of a portion of an IC (a two-level logic gate) having a dual gate FET.

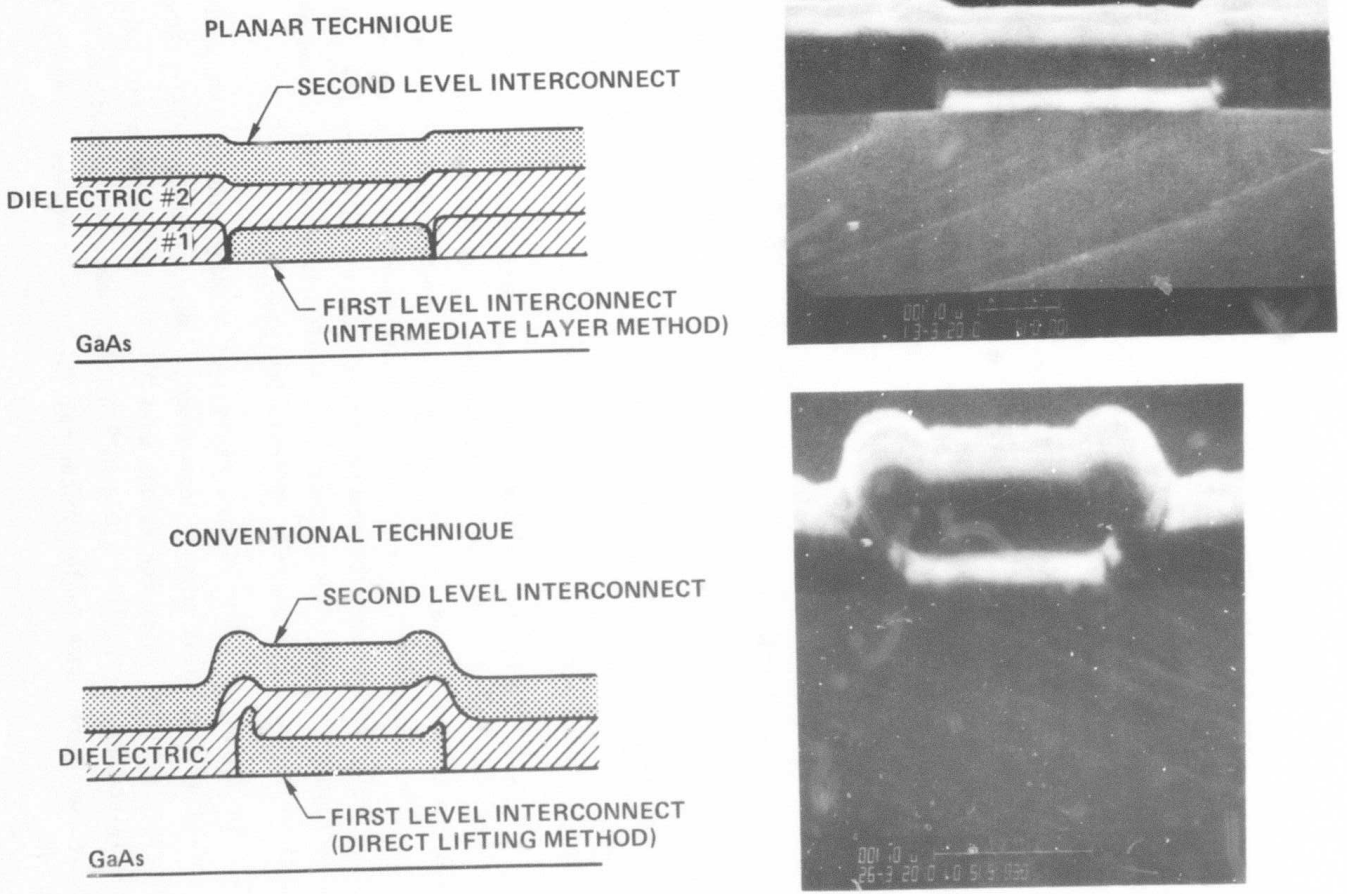

Fig. 4.3-5 Multi-level interconnect techniques comparing the planar Rockwell process with a conventional one.

Ohmic Contact and Schottky Barrier Processes

The reliability and quality of ohmic contacts in GaAs integrated circuits is a critical element directly influencing circuit performance. Low resistance ohmic contacts at the source and drain of FETs and at the cathodes of Schottky barrier diodes are difficult to attain because of the emphasis placed on high sheet resistance layers and small dimensions such as 10 μm FET widths and 1 μm x 2 μm Schottky barrier diode areas. Therefore, ohmic contacts are and will continue to be a subject of constant analysis and improvement.

Metallurgical ohmic contacts to GaAs are formed by melting a eutectic alloy composed of 88% Au and 12% Ge covered with a thin platinum overlay. A shallow surface layer of GaAs is dissolved during alloying of the AuGe film and immediately regrown upon subsequent cooling. The dopant (Ge) is incorporated in the epitaxially regrown GaAs forming a heavily doped layer. The current AuGe/Pt ohmic contact fabrication process consists of the following steps: a 1300Å film of AuGe is deposited and covered with a 300Å Pt layer; alloying is accomplished using a tube furnace with a hydrogen atmosphere, where the samples are exposed to a temperature between 450°C and 470°C for ~ 3 min. The contact metallization thickness, and the time and temperature for this process have been determined by experimental optimization.

During this program, the quality of the ohmic contacts has been continuously monitored. The ohmic contacts are probed on every wafer immediately after the alloying cycle in order to routinely monitor their quality. This measurement is made on a test structure employing gaps of several widths in order to subtract the channel resistance and calculate the specific ohmic contact resistance (TLM method). For a discussion on the TLM method and description of the test structure refer to Section 5.2.

The survey of ohmic contact resistance on many GaAs IC wafers over a long period of time shows gradual improvement. Approximately 1-1/2 years ago the average specific resistance values were $2 - 6 \times 10^{-5}$ Ω cm^2 while the current average values are typically $2 - 6 \times 10^{-6}$ Ω cm^2. Ohmic contact values below 10^{-5} Ω cm^2 are considered acceptable for current MSI level circuits. However, an area

for further analysis is the full determination of the performance trade-offs for ohmic contacts. In the early planning stage of the current program, it was thought that a third, n^{++}, implant step under all ohmic contacts would be required for good IC operation. This has not been necessary, and with the ohmic contact improvements in this program, the need for establishing an extra n^{++} implant step became questionable and was given a low priority. However, comparison of GaAs ICs with and without heavy doping under ohmic contact regions should still be undertaken. Reliability studies may ultimately determine the merit of using heavily doped degenerate regions under ohmic contacts.

4.4 Multi-Level Interconnects

In order to obtain high yields on very high density LSI/VLSI cicuits, a refined multilevel interconnect process is required. A dry etched, multi-level interconnect process which is LSI compatible has been under development in this program. Important features of this process include a unique planar crossover structure, the use of high quality plasma Si_3N_4 dielectric, and reactive ion etching and ion milling for pattern replication.

The planar GaAs multi-level interconnect process follows the fabrication step when the first level metal was deposited within plasma etched windows of the first level dielectric at a thickness equal to the thickness of the first level dielectric (Section 4.3). The 2nd level metal process starts with the deposition of plasma silicon nitride over the entire wafer. Via openings are then reactively ion etched through the Si_3N_4 for interconnecting the first level metal to the second level metal. The second level metal is deposited over the plasma silicon nitride, while it also fills the via windows. The second level interconnects are then defined by ion milling. This results in a planar structure that greatly enhances the yield of the multi-level interconnect process. Figure 4.4-1 is a schematic comparing the Rockwell planar multi-level interconnect approach with a conventional IC approach. The key feature of the Rockwell approach is the smooth planar crossover structure. This unique structure eliminates potential crossover problems such as shorts between first and second level metal interconnects and/or opens resulting from poor step coverage.

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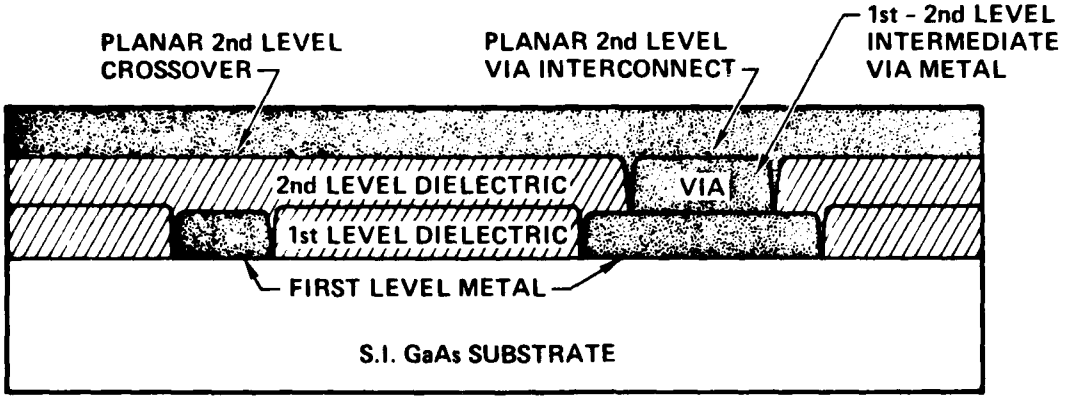
ROCKWELL PLANAR
MULTI-LEVEL INTERCONNECT STRUCTURE



CONVENTIONAL
MULTI-LEVEL INTERCONNECT STRUCTURE

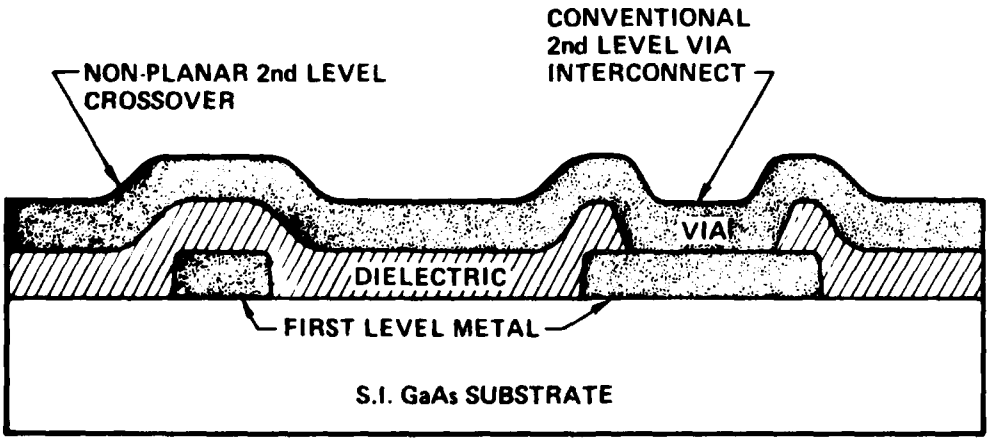


Fig. 4.4-1 Super planar vs conventional multi-level interconnect approach showing the planar crossovers as well as the planar via hole structure.

Another advantage of this approach is that during the 2nd level interconnect processes the critical GaAs MESFET channel surface region between the gate and source-drain contacts is protected by the first level dielectric. This surface protection contributes to the high yield of low pinchoff voltage devices ($V_p \approx$ 1.0 V) utilized in low power digital ICs. As shown in Fig. 4.4-1 the process can be further refined by filling with metal the via windows interconnecting the 1st and 2nd level of metallization. This filling can be easily accomplished using a process similar to the first layer metal process described in Section 4.3. Such refinement is capable of providing a fully planar via interconnect structure.

In the following, the various processes, and development activities associated with GaAs planar multi-level interconnects are discussed in detail.

Second Level Dielectric

The dielectric layer which serves as insulation between the first and second level metal must be a low stress, pinhole free layer with good adherence to metals, GaAs, and other dielectrics. The deposition process must not cause any thermal or electric damage to the devices, and the dielectric must be easily etched for via openings. All of these requirements are satisfied by plasma silicon nitride. The techniques employed to deposit plasma silicon nitride are similar to those described by Gereth and Scherber.[24] The resulting films are pinhole free over 10^{-3} cm^2 test areas with a crossover capacitance per unit area of 1.42×10^{-8} F/cm^2 for 5000Å thick films. The average dielectric constant of the plasma Si_3N_4 films is ~ 8. In contrast, bulk Si_3N_4 has a dielectric constant of 8.5, and high quality dense Si_3N_4 deposited by reactive sputtering has a dielectric constant of 6.4, while plasma deposited SiO_2 has a dielectric constant of 4.2.

Capacitances of typical crossover geometries calculated for the current plasma nitride process are tabulated in Table 4.4-1. In order to minimize the crossover capacitance for maximum operating speed, the use of dielectric films with lower relative dielectric constants should be considered. Continued

Table 4.4-1
Capacitances of Typical Crossover Geometries Calculated for the Current Plasma Nitride Process

Crossover Type	Crossover Linewidth Area	Capacitance t = 5000 Å ε = 8
Signal line over Signal line	1.5 μm x 1.5 μm 2.25 μm^2	0.32fF
Signal line over Power supply line	1.5 μm x (3-5 μm) 4.5-7.5 μm^2	0.64-1.1fF
Power supply line over Power supply line	(3-5 μm) x (3-5 μm) 9-25 μm^2	1.3-3.6fF

process development is needed to evaluate whether lower dielectric constant films can meet all of the necessary criteria for second level dielectric.

Via Window Etching

Via openings required for connecting the first level interconnects to the second level interconnects are opened by reactive ion etching (RIE). The first level metal (Au) serves as an automatic etch stop; it also provides excellent adherence to the second level metal since a small amount of Au is sputtered during the RIE process.

The reactive ion etching of plasma nitride can be tailord to produce isotropic or anisotropic etched profiles depending on the plasma etching paramaters used. Currently isotropic etching is used; the sidewall of the etched vias are sloped as shown in Fig. 4.4-2(a). In conventional processing, sloped holes are necessary since the current path between the second level metal and first level metal must pass over the sidewalls of the via. The yield and reliability

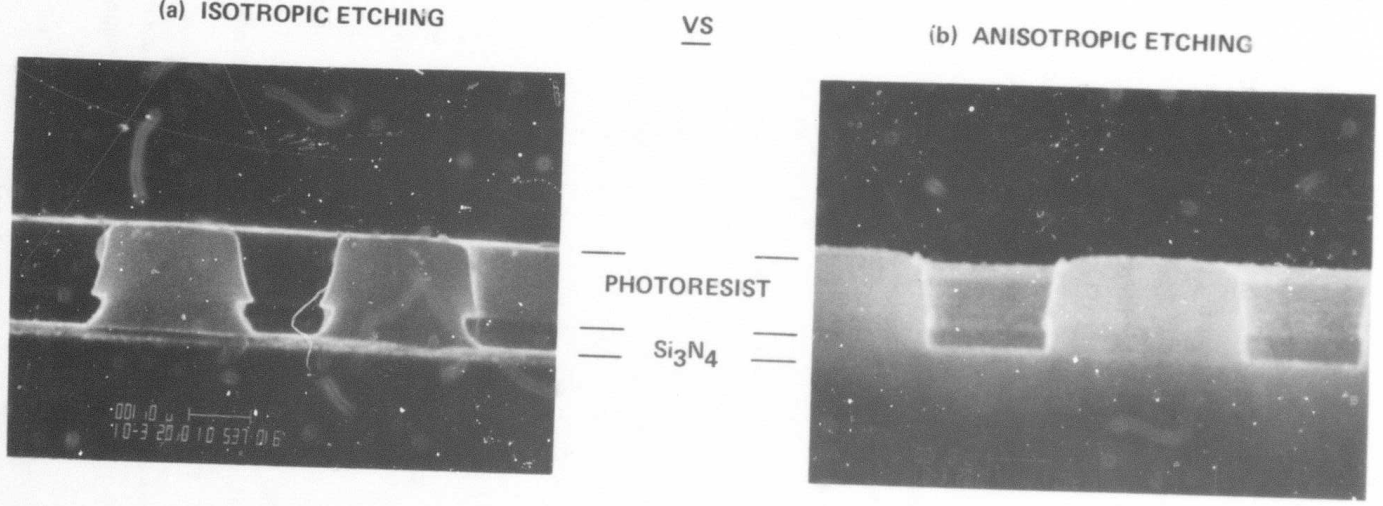


Fig. 4.4-2 Scanning electron micrograph of the reactive ion etched plasma nitride (5000A thick) before the removal of the photoresist; (a) isotropic etching; (b) anisotropic etching.

of the interconnect depends on the integrity of the sidewall coverage. Planetary e-beam evaporation or magnetron sputtering is used to ensure good metal sidewall coverage. The disadvantage of using a 60° isotropic sidewall via slope is that a 1 μm x1 μm interconnect to the first level metal requires the top of a 5000Å thick 2nd level dielectric to be 1.5 μm x 1.5 μm. Therefore the dimensions of via holes are actually larger than needed when isotropic profiles are used. With a 0.5 μm alignment tolerance, the second level metal has to be at least 2.5 μm wide to cover a 1 μm x1 μm via. Although this is a workable approach, it is rather detrimental to the circuit density required for LSI.

Anisotropic etching of via windows has been developed. Figure 4.4-2(b) shows an anisotropically etched via hole with nearly vertical dielectric sidewalls and negligible under-cut. Intermediate via hole metal is defined by depositing a metal film of slightly less thickness than the second level dielectric, followed by a lift-off process. This process scheme results in a planar structure as shown in Fig. 4.4-3. Sidewall coverage is no longer necessary for a filled via, hence the yield and reliability of second level metal to first level metal interconnects can be much higher when this approach is used. Since the via does not have any under cut (anisotropic) and there is no step coverage, a denser second level interconnect is possible. This unique via approach is promising for ultra dense, high yield LSI/VLSI circuit.

Ion Milling Pattern Replication

Chemical etching of the second level metal was not considered an acceptable method because of the fine line requirements of GaAs ICs. Several dry etching techniques were considered, including ion milling, sputter etching, reactive ion etching, and plasma etching. Ion milling was chosen because it was a field and plasma free process, and it was conducted in a high vacuum environment. In addition, ion milling is not a chemical process, and any material can be etched without difficulty.

A Commonwealth Scientific Millatron II is used for ion milling at a pressure of 1.5×10^{-4} Torr or lower. Samples are mounted on a water cooled

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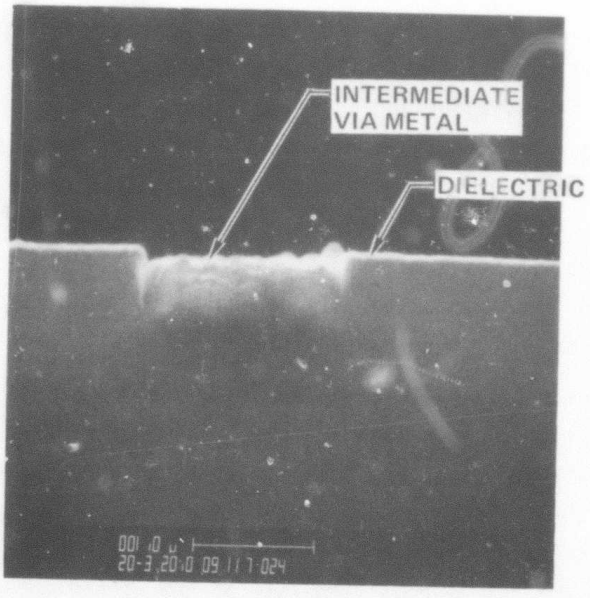


Fig. 4.4-3 Scanning electron micrograph of the cross section of an anisotropically etched and then filled via window.

stage which can be rotated around its axis, and simultaneously translated back and forth along the stage plane. The rotation assures that no shadowing or buildup of surface defects will occur as a result of unidirectional milling. The translation tends to average out nonuniformities in ion beam current density. The type of ion beam selected, along with the current, energy and angle of incidence, can be chosen independently for any given application. The beam reaching the substrate can be electrically neutralized, so that surfaces do not become positively charged repelling or distorting the ion beam.

Angle of incidence is an important parameter in ion milling. It can be selected to give either the maximum etch rate or the maximum differential etch rate for a particular pair of materials. The etch rate of Au, Ti, Si_3N_4, GaAs and photoresist at various angles of incidence are shown in Fig. 4.4-4. The angle of incidence is measured between the incident ion beam and the substrate surface plane. All of the materials of interest, except Au, have low etch rates at 90° incidence. In general the etch rate increases when the angle of incidence is reduced, and reaches a maximum at an angle of ~ 40°. It later decreases as glancing angles are approached. In contrast, the etch rate of Au is the highest at 90° incidence, and it decreases monotonically with reduced incidence angle.

The etch rate ratio of Au to Si_3N_4 reaches a maximum at a 90° angle of incidence. This indicates that the short extra milling period, which is necessary to ensure that metals are completely etched through, will not etch the Si_3N_4 to any great degree provided a 90° angle of incidence is used. However, the angle of incidence cannot be freely chosen for maximum differential etch rates because the net redeposition rate of the etched materials also depends on the angle of incidence. Redeposition, often observed along the edges of photoresist patterns, consists of ridges of metal left behind after the resist pattern is removed (see Fig. 4.4-5a). The redeposited material is undesirable because it could create shorts between isolated metal lines, or it might prevent complete coverage by a subsequently deposited dielectric layer. The material is redeposited on the sidewalls of the photoresist pattern at glancing angle with respect to the incident ion beam. If a 90° incidence angle is used for best

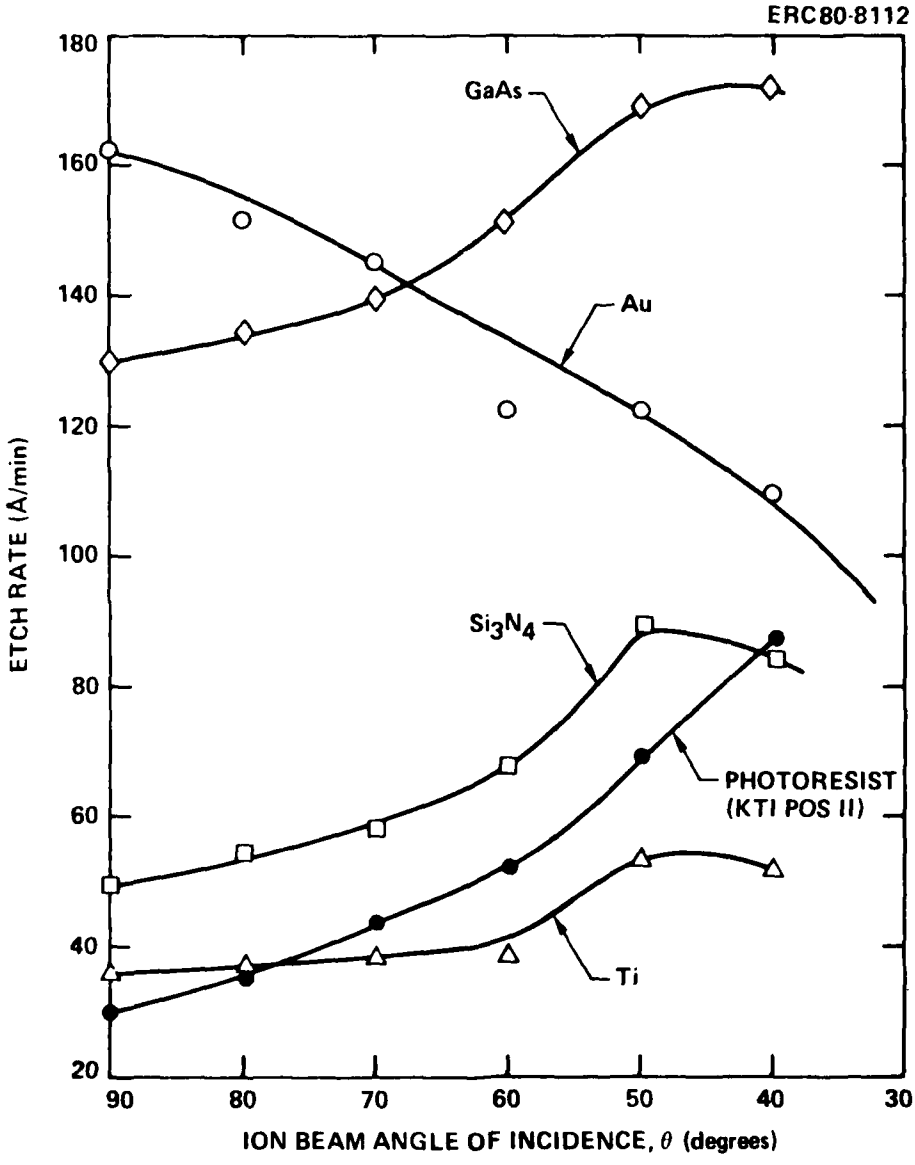
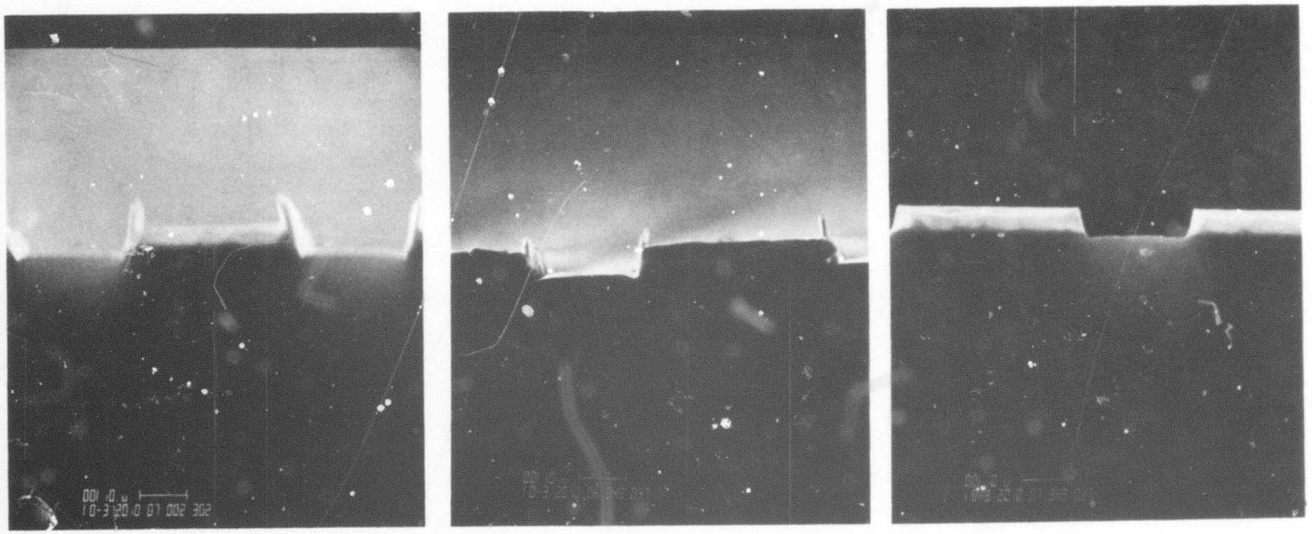


Fig. 4.4-4 Etch rate vs angle of incidence for ion milling.



(a) (b) (c)

Fig. 4.4-5 Experimental results of ion beam etching of 300Å Ti/5000Å Au at various incidence angle θ. (a) θ = 90°, (b) θ = 80°, (c) θ = 70°.

etch stop (maximum differential etch rate) the redeposited material forms ridges to the height of the photoresist. This is shown in the scanning electron micrographs of Fig. 4.4-5(a).

One solution to the redeposition problem is to tilt the ion beam. An off-normal ion beam will simultaneously etch away the material as it is redeposited on the sidewall of photoresist. When an optimized incidence angle is used, the net redeposition rate can be zero, and a nearly vertical wall of the etched pattern can be obtained (Fig. 4.4-5(c)). Illustrated in Fig. 4.4-5(a), (b) and (c) are SEM photographs of samples etched at three different incidence angles (θ = 90°, 80°, 70°). This data show that the ridge height of the redeposited material decreases with increased tilt of the beam angle. At an incidence angle of 70° there is no redeposited ridge and the etched pattern has a reasonable vertical edge. Therefore, a 70° incidence angle is currently used for ion milling, minimizing redeposition effects.

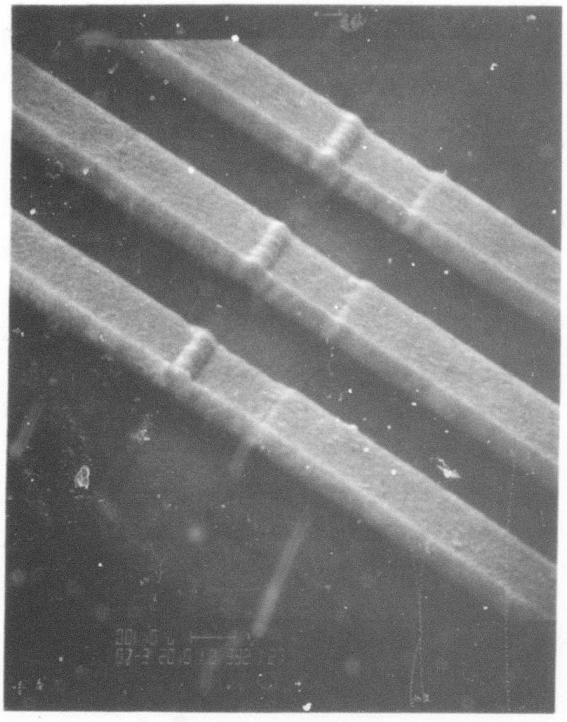
The currently used ion milling technique is reproducible, and it has resulted in excellent yield for delineating the second level metal. However, several elements of the process still need to be refined. Unlike the plasma etching of Si_3N_4 via windows, which stops automatically at the underlying Au, the ion milling process must be terminated manually when the unmasked metal film has been etched off completely. This is currently done by knowing the metal film thickness and etching rate, and estimating the time required to etch off the metal film. More reliable end-point detection methods, such as mass spectroscopy, are under consideration.

Planar Multi-Level Interconnect Results

The upper portion of Fig. 4.3-5 shows the smooth planar crossovers resulting from the planar multi-layer fabrication approach. The planar crossovers eliminate any potential for problems such as shorts between first and second level interconnects, and high resistances or open interconnects resulting from poor step coverage. An example of ion milled planar second level interconnects is shown in Fig. 4.4-6. With this dry etching technique, precise linewidth

SC79-5893

GaAs IC
PLANAR CROSSOVER



PROCESS

METAL REPLICATION
ION MILLED

SECOND LEVEL METAL
5500Å TiAu

SECOND LEVEL DIELECTRIC
5000Å PLASMA NITRIDE

Fig. 4.4-6 SEM photograph of a portion of a planar IC showing the almost total lack of steps at metallization crossovers.

control with near vertical walls can be maintained for Ti/Au films up to 1 μm thick.

Figure 4.4-7 shows a very compact GaAs IC that utilizes, for the sake of density, parallel first-to-second level crossovers. The ability to accommodate this type of circuit layout without compromising process yield or circuit performance demonstrates the power of this planar crossover approach. Furthermore, this planar multi-level interonnect structure provides, in principle, the capability for fabricating more than two levels of interconnects.

The reliability of Rockwell low thereshold MESFETs during multilevel interconnect fabrication is a good test of the overall process integrity since the surfaces are exposed to elevated temperature (~ 250°C plasma nitride deposition), and to the influence of reactive ion etching and ion milling. Test FETs are routinely monitored before and after the second metalization process. Figure 4.4-8 presents a pinch-off voltages of 72 such devices uniformly distributed over a wafer measured before and after the multilevel interconnect process. The average shift of pinch-off voltage, $\Delta\bar{V}_p$, after the multi-level interconnect process is only 51 mV. This negligible change indicates that the process is quite acceptable for low pinchoff voltage devices (V_p = 1.03 V in this example).

It has also been observed that the saturation current of the test FETs decreases slightly after the second level metal process. Possible causes for these changes may be related to the additional stress from the second level dielectric (plasma nitride) and/or possible degradation of ohmic contacts. Further investigations into all reliability aspects of the planar GaAs IC process will be carried out in the future.

In summary, a high yield, dry etched multi-level interconnect process has been developed. A high quality, low stress plasma silicon nitride film is used to electrically isolate the first level metal from the second level metal. Reactive ion etching is used to etch via openings and ion milling is used to delineate the second level interconnect. With these two dry etching techniques the size of etched features is limited by lithography only. These techniques, along with the planar structure utilized, make the process very promising for realizing high yield digital GaAs LSI/VLSI structures.

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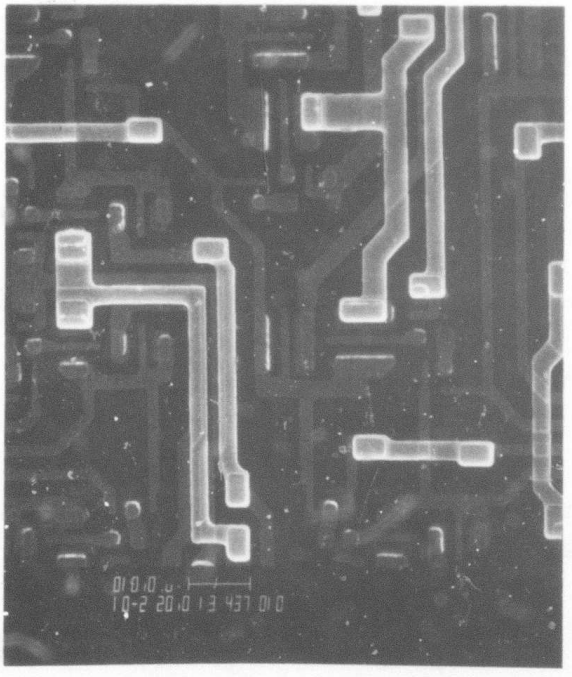

Fig. 4.4-7 A SEM photograph of a portion of a planar IC showing excellent lithography and high density. Note the second level interconnects running parallel above first level interconnects.

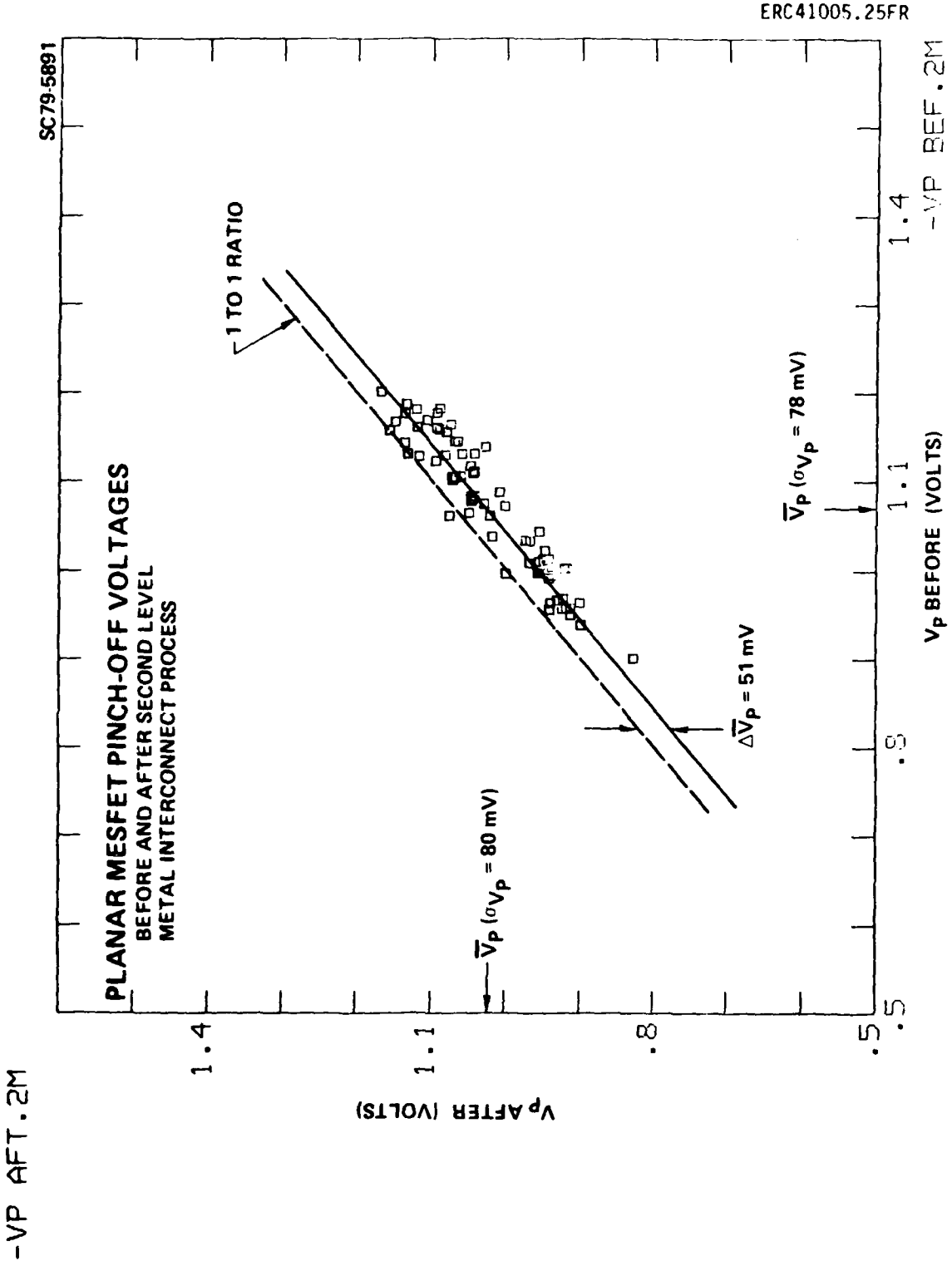

Fig. 4.4-8 Pinchoff voltage of test FET on a GaAs IC wafer before and after the second layer metallization process.

4.5 Planar IC Process Capability and Yield

Progress made during the first two phases of this program represents significant advances in processing techniques, leading to a planar "silicon-like" fabrication technology, and making possible the fabrication of complex GaAs ICs. The advances have centered around the use of multiple localized ion implantations, high yield circuit lithography techniques, and a unique planar multi-level interconnect structure (discussed in previous sections).

IC fabrication yields using this process have been good. GaAs ICs such as the 5 x 5 bit parallel multiplier (260 gates) discussed in Sec. 6.4 have been fabricated with good yield and excellent performance. Circuits with 1000 gates (8 × 8 bit parallel multiplier) have been fabricated and tested showing almost complete operation. Although the GaAs process capability has been clearly demonstrated, some considerations on yield are in order.

In a research oriented process development program such as this, unambiguous yield information cannot easily be established. Some yield assessment can be made by factoring yield into two categories: yield of good processed wafers; and yield of operational circuits within a good wafer. The discussion in this section is restricted to yield of processed wafers.

A summary of the ARPA program wafer processing statistics in terms of mask sets, circuit complexity, wafer and ingot quantities, processing period, and processing yields is presented in Table 4.5-1. This table addresses processing yield in a reasonably quantitative manner while also showing the relative degree of complexity of each mask set used during the program. The statistics presented in Table 4.5-1 include all the wafers started in the planar GaAs IC process specifically for evaluating circuit designs, processing planar ICs and evaluating their performance. Other fragmented wafer processing work primarily in process development tasks is not represented. The comments will focus on mask sets AR1 to AR5. Early work on contact mask ICFET will not be discussed since this work was preliminary and low in volume.

The general conclusion reached from Table 4.5-1 is that good progress has been made during this program. However, it is very difficult to precisely

Table 4.5-1

Planar GaAs IC Process Technology
Wafer Processing Statistics

ERC80-9712

MASK SET	ICFET	AR1	AR2	AR3	AR4	AR5
PROCESS APPROACH	CONTACT 1-IMPLANT	4X PROJECTION PHOTOLITHOGRAPHY MULTIPLE LOCALIZED IMPLANTS				
CIRCUIT	NOR GATE	RING OSCILLATORS	DIVIDERS MULTIPLEXER	3 x 3 MULTIPLIER	5 x 5 MULTIPLIER	8 x 8 MULTIPLIER
COMPLEXITY	1 GATE	7-9 GATES	25-67 GATES	75 GATES	260 GATES	1008 GATES
PROCESSING PERIOD	7/77-9/77	10/77-6/78	7/78-3/79	4/79-11/79	11/79-6/80	5/80-6/80
#WAFERS	8	28	32	28	28	20**
#INGOTS	1 HB	4 HB	4 HB	4 HB	5 HB 1 LEC	4 HB
MISC. YIELD						
BREAKAGE	—	21/28 (75%)	30/32 (94%)	23/28 (82%)	26/28 (93%)	15/16 (94%)
OHMIC CONTACT	—	75%	93%	92%	100%	100%
ISOLATION	—	100%	~90% 1 BAD INGOT	100%	100%	100%
FIRST LEVEL						
COMPLETED	—	19/28 (68%) *(83%)	24/32 (75%) *(80%)	23/28 (82%) *(92%)	28/28 (100%) *(100%)	15/16 (94%) *(100%)
PASSED dc TEST	—	9/19 (47%)	16/24 (67%)	16/23 (70%)	25/28 (89%)	15/15 (100%)
SECOND LEVEL						
COMPLETED	—	9/9 (100%)	16/16 (100%)	14/16 (88%)	21/21 (100%)	8/8†† (100%)
OVERALL YIELD FULL PROCESS	—	9/28 (32%) *(43%)	16/32 (50%) *(53%)	14/28 (50%) *(61%)	21/28 (75%) *(78%)	
YIELD HI SPEED DYNAMIC TEST	—	4/9 (44%)	7/13 †(54%)	4/9† (44%)	3/5 ☆(60%)	IN TEST

*ADJUSTED FOR WAFER BREAKAGE
**NUMBER OF WAFERS STARTED, 8 WAFERS FINISHED
†ADJUSTED FOR WAFERS NOT TESTED
☆14 WAFERS PROCESSED WITH DEFECTIVE SCHOTTKY MASK LEVEL
††7 WAFERS STILL IN SECOND LEVEL PROCESS

44% INCREASE IN CIRCUIT AREA

measure and compare this progress since each successive mask set included new, more complex GaAs ICs. Some general observations can be made. A reasonable quantity of wafers (28 - 32) and a variety of GaAs ingots (> 4 each) have been used on each mask set. Using ~ 20 different ingots in total on AR1, AR2, AR3, AR4, and AR5 with good success, clearly indicates that the reliance of the planar approach on device isolation provided directly from GaAs semi-insulating substrates is sound, and is not dependent on certain "magic" ingots. Processing almost 150 wafers has resulted in only ~ 3 wafers, all from the same ingot, with clear device isolation problems. The initial substrate qualification on this particular ingot gave marginal results. Consequently, this result was not unexpected. The conclusion from the data is that 100% of the wafers have good isolation provided the GaAs ingots are properly qualified.

Ohmic contact yield statistics are included in this table because it was an issue for concern during the initial stages of the process development. After starting with 75% yield on AR1, 90 - 100% ohmic contact process yields have been experienced on subsequent mask sets. (100% yield on ohmic contacts implies that acceptable ohmic contact values in terms of providing good circuit performance are achieved.) As shown in the table, wafer breakage varies widely, and is not easy to interpret. It is anticipated that overall GaAs wafer breakage may average between 10 to 15%. In Table 4.5-1 both the absolute yields and yields adjusted for wafer breakage are given.

The statistics on the lower half of Table 4.5-1 show significant progress in process yield during the current program. For example, on mask AR1 only 68% of the wafers (83% when adjusted for wafer breakage) reached the first level metal dc testing stage, while on the two most recent masks all or almost all of the wafers (100% and 94% respectively) reached the dc test stage. As can be seen in the table, gradual improvement has taken place on all fabrication stages. A meaningful perspective of fabrication improvement is given by the increasing percentages of wafers passing dc testing (47% for AR1, 67% for AR2, 70% for AR3, 89% for AR4, and 100% for AR5). This steady improvement has taken place despite gradual tightening of test standards for acceptance at dc

testing. Parallel progress in yields of wafers completed through the full process (including 2nd level interconnects) has been observed, with yields increasing from 43% on AR1, to 53% on AR2, 61% on AR3, and 78% on AR4. While excellent wafer process yield does not guarantee good yield on working devices, it is certainly an indication of the overall material and process improvement. In practice, such improvement should correlate well with increased yield of working ICs. In summary, significant progress in process throughput, quality and yield, have been shown while circuit complexities have increased from SSI/MSI to the LSI level.

5.0 PROCESS MONITORING AND STATISTICAL DATA

The development of a fabrication technology involving new materials and new circuit concepts requires a substantial investment in process monitoring and measurement techniques. In some of the more established silicon technologies, this process monitoring activity has acquired importance just recently, with efforts to scale down device dimensions. In the current planar GaAs IC technology program, a strong effort was made from the outset to acquire larger quantities of statistical information by process monitoring techniques.

The importance assigned to process monitoring techniques is reflected in the amount of wafer area assigned to process monitoring. This is illustrated in Fig. 5.0-1, a schematic of a wafer from mask set AR3. Two types of test areas, corresponding to two applications of the test structures are shown in the figure. A fairly dense array of test areas labelled T1/T2 contains test structures used for monitoring process and device uniformity. The high density of the array requires automatic testing techniques, so that large volumes of data can be easily gathered and displayed in statistical fashion. The second type of process monitoring area, labelled PM in Fig. 5.0-1, is a "drop in" chip surrounded by eight chips containing circuits. This chip contains a wide variety of test structures ranging from simple process monitoring test structures to more sophisticated test structures such as ring oscillators, device arrays, and experimental circuits.

In Section 5.1, the organizaton of the PM chip is discussed and the principal test structures are described and illustrated by data. In Section 5.2 the T1/T2 area is described. In Section 5.3 the automatic testing facility developed for the GaAs IC program is covered. In Section 5.4 statistical data from test devices are discussed.

5.1 The PM Chip. Process Control Test Structures

The PM chip (see Fig. 5.0-1) is relatively large (2.25 × 2.25 mm on mask sets AR1, AR2 and AR3 and 2.7 × 2.7 mm on AR4 and AR5), and is repeated four times over a wafer. Figure 5.1-1 is a photograph of this chip from a

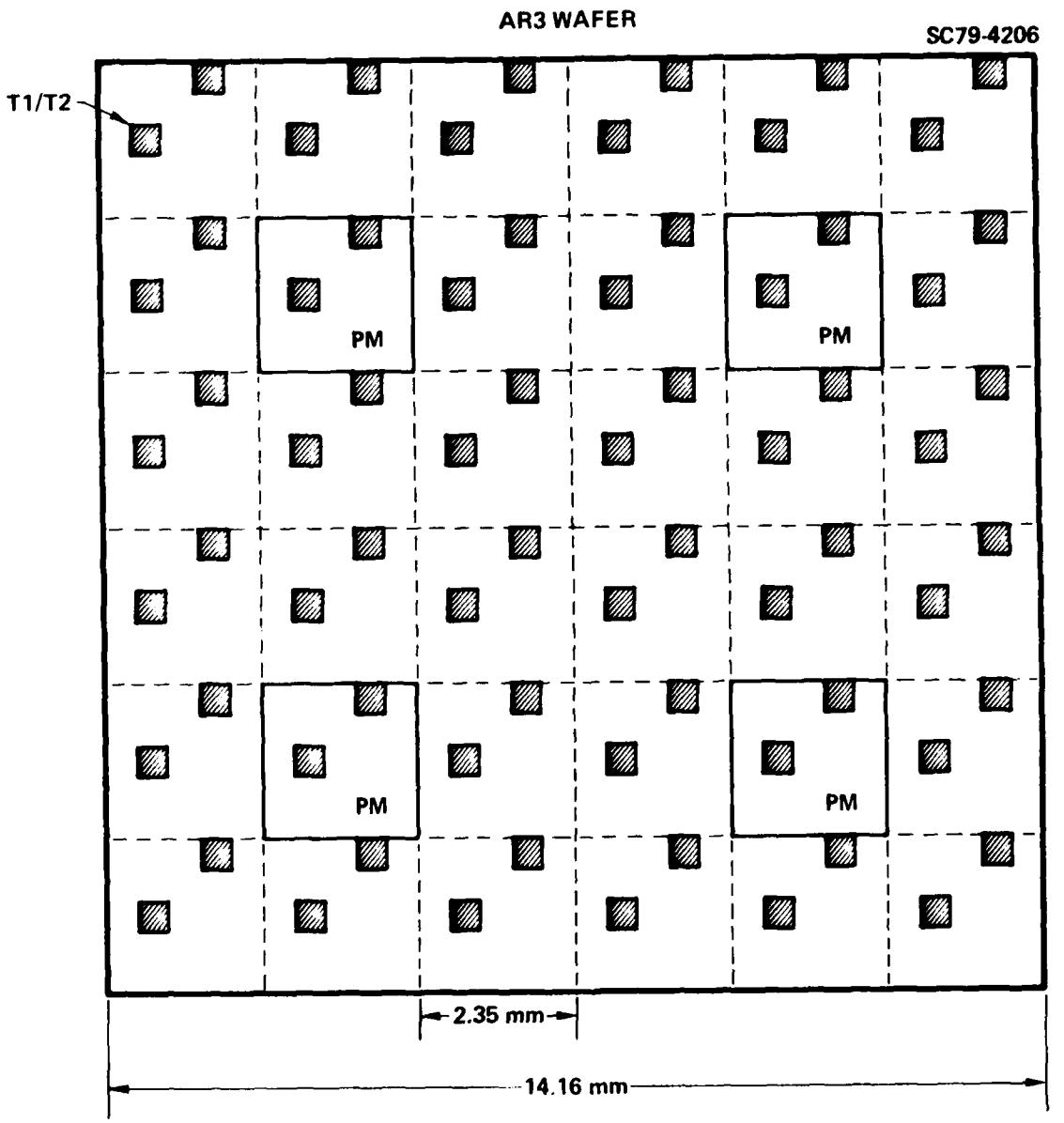

Fig. 5.0-1 Distribution of test areas over a wafer.

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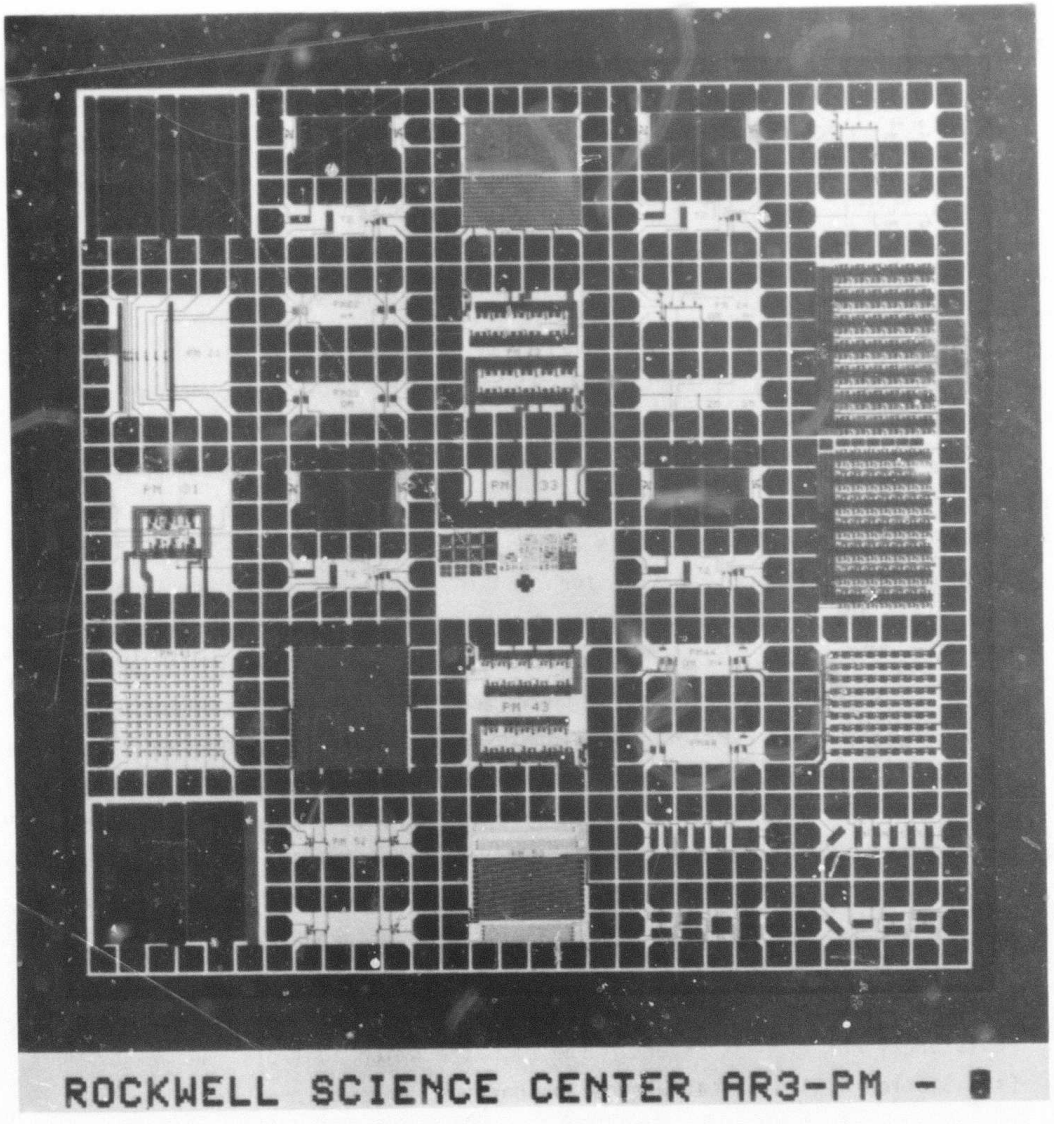

Fig. 5.1-1 Photograph of the process monitor (PM) chip for mask set AR3. The overall dimensions are 2.15 × 2.15 mm.

typical mask set, and Fig. 5.1-2 contains a map labeling the PM test structures. The test structures in this chip can be considered in two groups. The first group is used for tests for direct evaluation of individual fabrication steps, such as C-V test structures for carrier concentration profile measurements, metallization test structures, etc. The second group contains FET arrays, ring oscillators, and experiments on device and circuit design. This organization concept has remained unchanged through several mask sets, but the test structures for evaluation of fabrication steps have evolved as dictated by the experience from previous masks. The experimental test structures have varied even more radically from mask to mask as required by the development work. In the rest of this section, the most important test structures and some of the conclusions obtained from their utilization are discussed.

Monitoring of carrier concentration profiles for the shallow FET channel layers is essential in this planar low power GaAs technology. Although doping profiles are monitored on small test chips implanted in parallel with the wafers in process, and profiles are also indirectly checked through the measurement of pinchoff voltages of FETs, some evaluation of carrier concentration profiles on fabricated wafers is needed. This is done on the test structures labelled C-V in Fig. 5.1-2 (see for example, the upper and lower left corners). The PM chip contains one C-V test structure for each type of implant, n^-, n^+, and the combination of both (labeled $n^- + n^+$). The diodes used for these C-V measurements (measuring 50000 μm^2) have one ohmic contact on each side of a large Schottky barrier. Both ohmic contacts are tied together for C-V measurements. However, these ohmic contacts can also be treated as the source and drain of a "fat" FET which can then be used for measuring mobility profiles.[25] The basic equipment for the C-V measurements consists of a current amplifier and a lock-in detector to measure the capacitive component of the ac current through the diode. The measurement is normally made at a frequency of 10 kHz. This frequency is lower than the conventional 1 MHz frequency, to avoid series resistance limitations, which can be appreciable for the very shallow (high sheet resistance) FET channel layers. The computer which controls the measurement (see Section 5.3) also calculates the carrier concentration profile.

MASK AR3
PM

SC79-4064

11 C - V n^-, n^+	12 T 1 / T 2	13 OVERCROSSING INTER-CONNECTS	14 T 1 / T 2	15 NBS ALIGNMENT Ω/n^+ Ω/SM
21 VOLTAGE PROBE	22 FET INTERACTIONS	23 10μm RING OSCILLATOR	24 NBS ALIGNMENT Ω/n^- 2M/SM	25 LONG CHAIN 10μm
31 D - FF	32 T 1 / T 2	33 CONTACT RESISTANCE / RESOLUTION TARGETS	34 T 1 / T 2	35 LONG CHAIN 5μm
41 DIODE ARRAY	42 SM + 2M LINE RESISTANCE / CONTACT RESISTANCE	43 3μm, 5μm RING OSCILLATORS	44 GATE DESIGN	45 FET ARRAY
51 C - V n^- + n^+ MOM	52 NBS SHEET RESISTANCE AND LINEWIDTH	53 SM, 2M LINE RESISTANCE	54 VARIABLE GATE FETs	55 MISALIGNED FETS

Fig. 5.1-2 Map showing the distribution of test pattern on the PM chip of mask set AR3 (compare with Fig. 3.4-2).

Figure 5.1-3 shows a carrier concentration profile measured with the automatic test system. Superimposed on the C-V profile is a mobility profile obtained by combining the result of the C-V measurement with data from a measurement of channel conductance as a function of gate voltage (device transconductance) for the "fat" FET. The measurement is made at very small drain voltage (5 mV) to keep the electric field in the channel small, so that the depletion layer width does not vary appreciably from source to drain. The calculation of the mobility is described in Ref. 25. As shown in Fig. 5.1-3, the mobility in the channel varies with doping concentration, and it ranges between 4000 and 5000 cm^2/Vs. These values are very typical for the implanted layers used in the GaAs digital ICs. When only carrier concentration profiles for the FET channel layer (n^-) are required, they are measured on the diode structure located in the T1 test area (see Sec. 5.2) which offers higher density for statistical analysis.

The test structure labeled MOM in the lower left corner of Fig. 5.1-2 resembles a C-V test structure, but it consists of a capacitor formed by layers of first and second level metals separated by the second level dielectric. This structure provides a good test for pinholes in this dielectric, and it provides a direct value for the overcrossing capacitance and a value for the dielectric constant of the second level dielectric (the thickness is estimated from deposition data).

Figure 5.1-4 illustrates the evolution of sheet resistance measurements over several mask sets. The figure on the upper right shows the classic Van der Pauw configuration used in the first mask set. The lower right figure shows a test structure developed by the National Bureau of Standards (NBS) for sheet resistance and linewidth measurements.[26] The NBS cross portion of this structure is used in the same way the Van der Pauw test structure is used, and the same equations apply to the calculation of sheet resistance.[26] Figure 5.1-4 shows data comparing the two types of test structures on neighboring locations on the same wafer showing that indeed they yield the same results. This test was done on mask set AR2. The bridge portion of the NBS test structure is used to calculate linewidth by comparison of resistance per unit length with sheet resistance. In this example, the n^+ implant line was implanted through a 3 μm

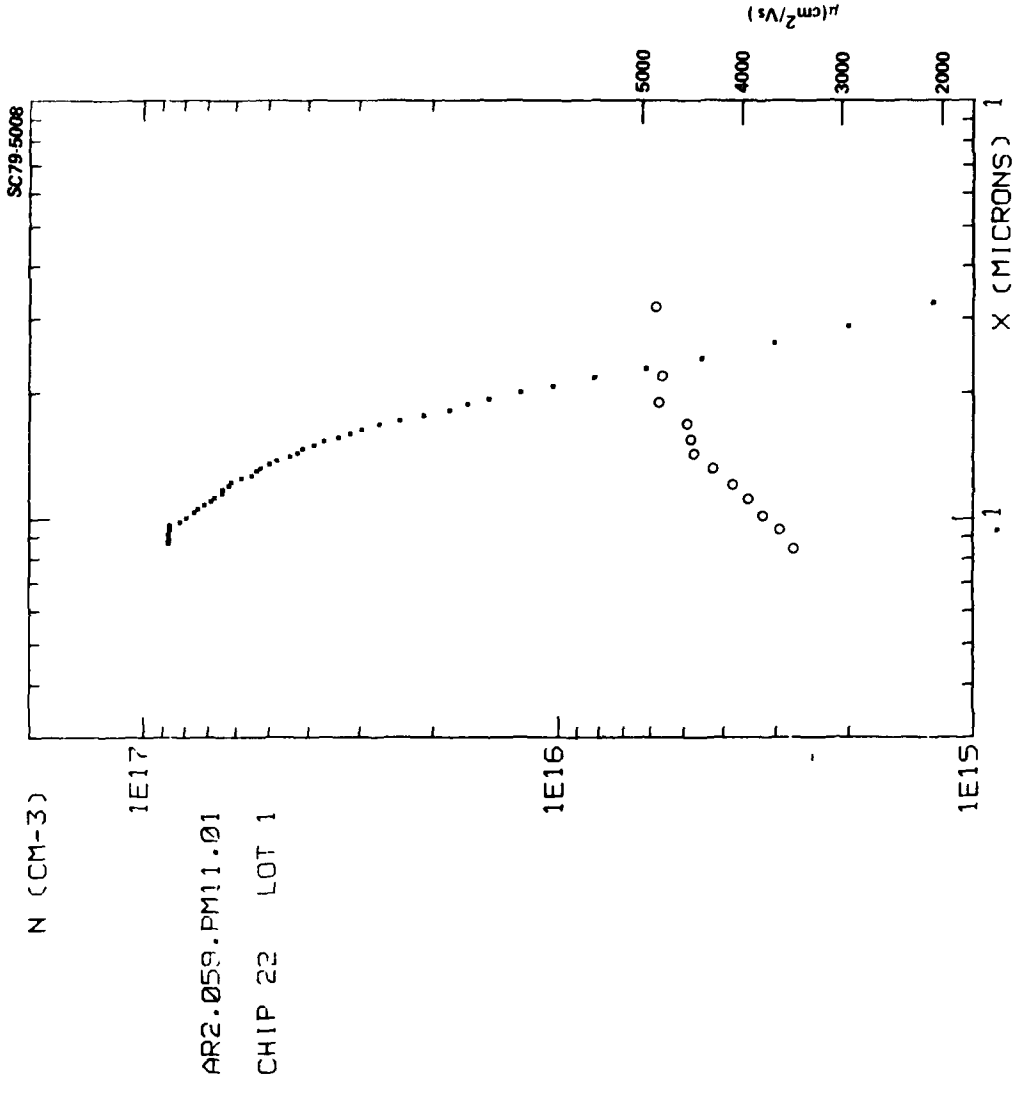

Fig. 5.1-3 Result of an on-chip measurement of mobility and carrier concentration profiles for a typical FET channel region.

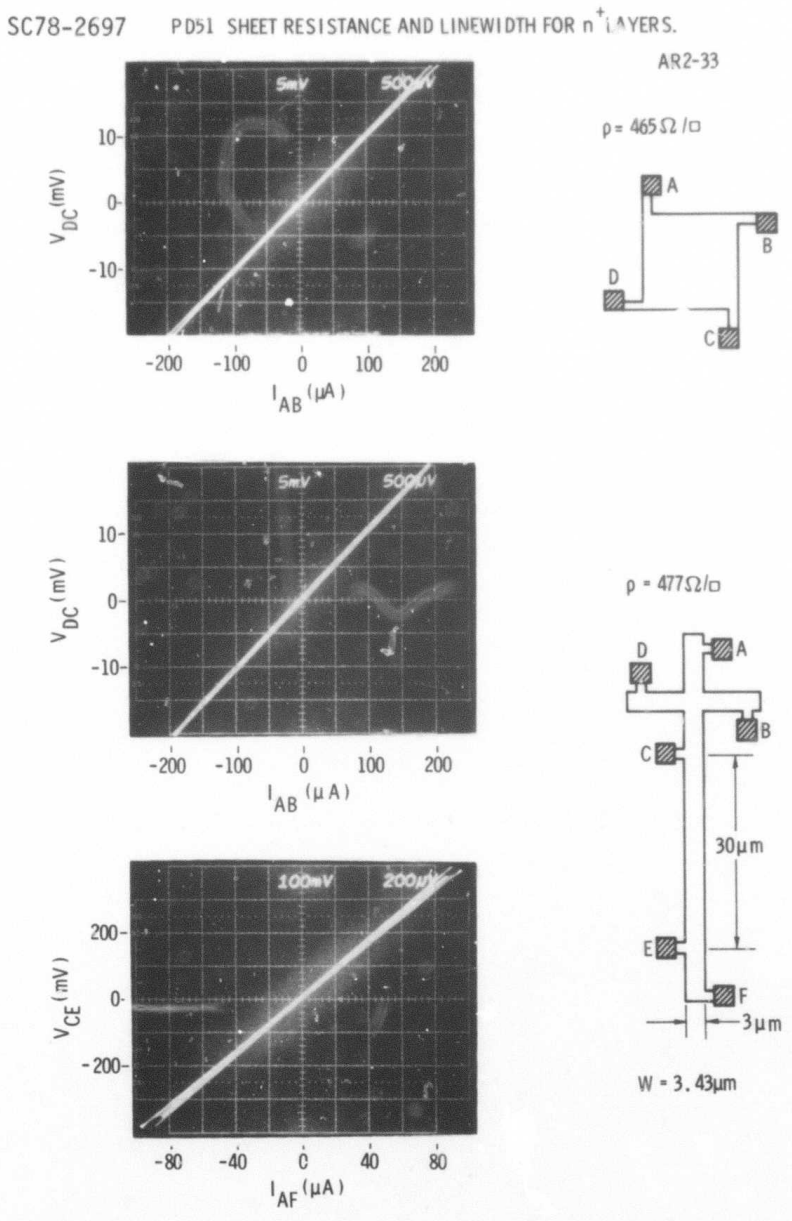

Fig. 5.1-4 Comparison of sheet resistance measurements using a conventional Van der Pauw pattern (top oscillogram) with an NBS cross test pattern (center). Also shown is the result of a linewidth measurement (bottom) using the bridge portion of the NBS test pattern.

wide mask. The measurement on the bridge portion of the structure indicates an effective width of 3.43 μm, due to the lateral diffusion of the sulfur implant during the annealing process. In view of its effectiveness and small dimensions the NBS test structure has been adopted in subsequent mask sets.

A number of test structures are used to monitor the metallizations (first and second layer) and their crossovers and interconnects. Long lines of several widths, with Kelvin connections at the ends to eliminate the effect of probe resistances, are used to monitor the sheet resistance of the metallizations (lot 53 of the PM chip in Figs. 5.1-1 and 5.1-2). This measurement is not needed frequently in view of the reproducibility of metal depositions, but it is sometimes required for diagnostic purposes. Metallization overcrossings are checked by a test structure consisting of a pattern of horizontal second layer metal lines crossing over a pattern of vertical first layer metal lines. A typical test structure has 600 crossovers (see upper half of area 13 in Figs. 5.1-1 and 5.1-2). The right portion of Fig. 5.1-5 shows an SEM photograph of a portion of such a test structure. The evaluation of the overcrossing test structure consists of checking for open lines or shorts between the two layers. This test structure, also a diagnostic type, is used very seldom due to the planarity of the structures (see Fig. 5.1-5), which have virtually no step to cover.

The interconnect test structure consists of a long chain of vias, typically 600, connected by first and second layer metal strips located on the lower half of area 13 (see Figs. 5.1-1 and 5.1-2). An SEM photograph of a portion of a similar test structure is shown on the left side of Fig. 5.1-5. This type of test structure was used in the first planar GaAs IC mask set to test the capability of the technology for small via dimensions. The vias showed on Fig. 5.1-5 measure only 1 × 1 μm, and yet good continuity was observed over a 600 via test structure on most wafers. Normally, a wide safety margin is allowed in the circuits by designing vias with 2 × 2 μm or 2 × 3 μm dimensions. The interconnect test structure on the recent masks was designed with these dimensions for routine after process measurement of the average via resistance. The main purpose of monitoring this resistance is to detect large increases above the typical values due to incomplete etching of the via windows or insufficient coverage

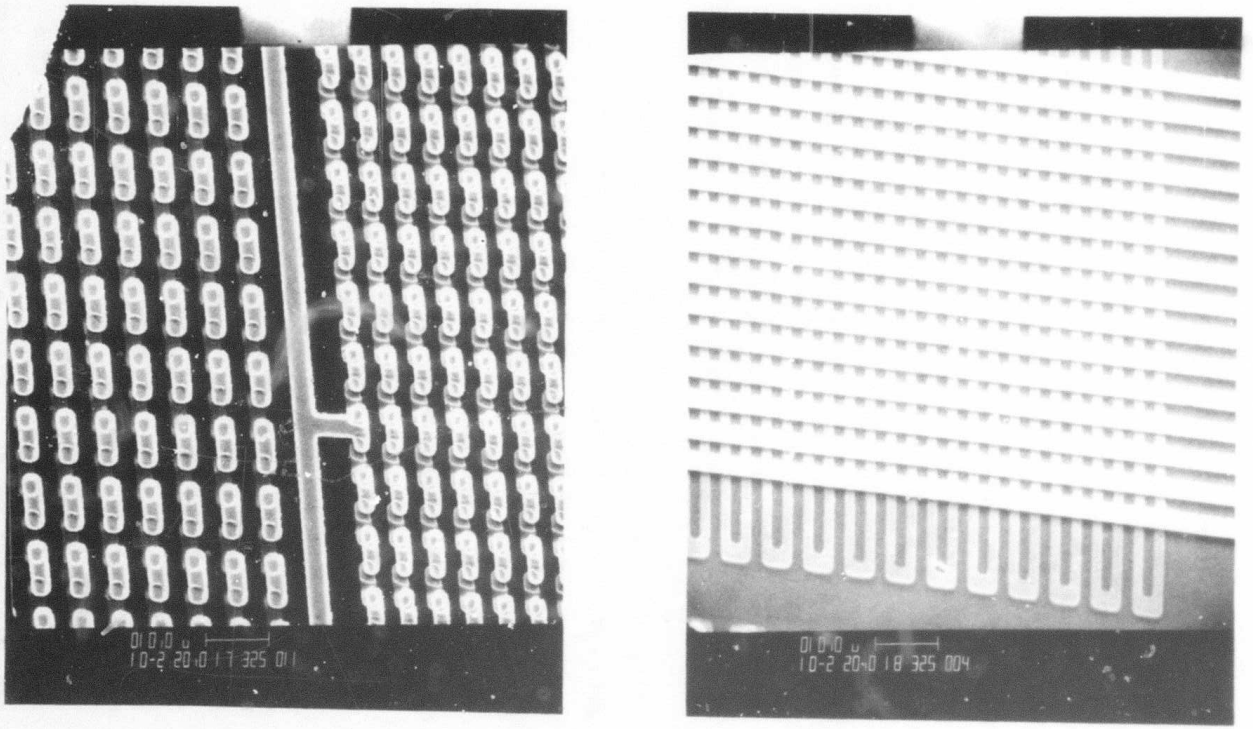

Fig. 5.1-5 SEM photograph of portions of interconnect and crossover test patterns. The interconnect test pattern (left) consists of a chain first to second level interconnects with vias measuring only 1 μm × 1 μm. Note the virtual lack of steps on the crossover test pattern (right) due to the planar structure.

of the walls of the via hole due to errors in second layer metallization thickness.

Test structures for electrical measurements of alignment between subsequent mask steps have been proposed.[27] The test structures are formed by aligning a contact in the center of a bridge built with a prior mask step, so that the unbalance caused by misalignment can be precisely determined with a potentiometric measurement. Although the concept is simple, and the measurement is very sensitive (it was tested on GaAs wafers in test areas 15 and 24 in Fig. 5.1-2), the electrical measurement can be made only between layers which make ohmic contact to one another. Therefore, the measurement is not suitable for the most critical alignment step in our planar fabrication technology, the alignment between the Schottky metal layer and the n^+ layer needed for correct placement of the FET gate in the center of the gap between the n^+ regions at the source and drain ohmic contacts. Visual inspection during fabrication provides a qualitative evaluation of the alignment, and quantitative measurements by optical techniques are feasible but very tedious. Therefore, an electrical evaluation tool is desirable. The possibility of forming diode structures with the Schottky metal layer and the n^+ layer so that measurements of current or sheet resistance unbalance can be used to calculate misalignment will be explored in future mask sets.

The PM chip provides an ideal place for experimentation in circuit design and in design rule development since the PM chips use only a moderate amount of total wafer area. Examples of such experiments are the study of the effect of orientation on FET characteristics (Section 3.4) Other examples of special test structures in PM are the FET array containing a 9 × 9 array of FETs, 20 μm wide, designed for the purpose of evaluating uniformity over a small area (Section 5.4), and long chains of gates consisting of 84 and 96 gates which were used for preliminary evaluation of MSI capability before high speed circuits with nearly 100 gates were implemented. Finally, some D-flip flop and ring oscillator circuits are usually placed in the PM chip to provide reference points on speed and power dissipation.

In the future, as the technology matures further, the experimental test structures will probably be eliminated. However, a significant reduction of the PM chip size is not expected because the crossover and interconnect test structures will need to be expanded in order to keep up with the increasing complexity of the circuits.

5.2 The T1/T2 Chip. Uniformity Control Test Patterns

The test areas labelled T1 and T2 in Fig. 5.0-1 consist of small, 440 × 440 μm, test cells containing the most critical process monitoring test structures and key devices. The number of cells is large (36 or 72), and the cells form a regular array over the wafer, so that process uniformity can be assessed. Plots of the T1 and T2 cells are shown in Fig. 5.2-1. The test structures in T1 are a diode for C-V measurements on the FET channel layer, n^-, two NBS sheet resistance test structures for the n^- and the n^+ (diode) layers,[26] a substrate isolation test structure, and test structures for ohmic contact evaluation.

The test structures for checking the isolation provided by unimplanted substrate areas have been reduced from a large assortment in the first mask sets to just one test structure in the current masks, a 3 μm gap between two 50 μm wide contacts. This reduction is due to the effectiveness of the substrate qualification procedures in screening substrates so that they do not form conductive layers in the unimplanted regions.

The ohmic contact test structures have undergone a sequence of improvements since the early masks, although the principle has not changed. The structure consists of several pairs of contacts placed on a conductive layer and separated by gaps of different lengths (currently 3, 6, and 9 and 12 μm). The resistance between each pair of contacts is measured, and the contact resistance is extrapolated from a resistance vs gap length plot. Despite its conceptual simplicity the implementation of this test is not straightforward because of the complex design of the ohmic contacts in our planar devices. The ohmic contact metal is alloyed in areas which are also implanted with an n^+ layer (in addition to the FET channel n^- implant) for low sheet resistance under the contacts.

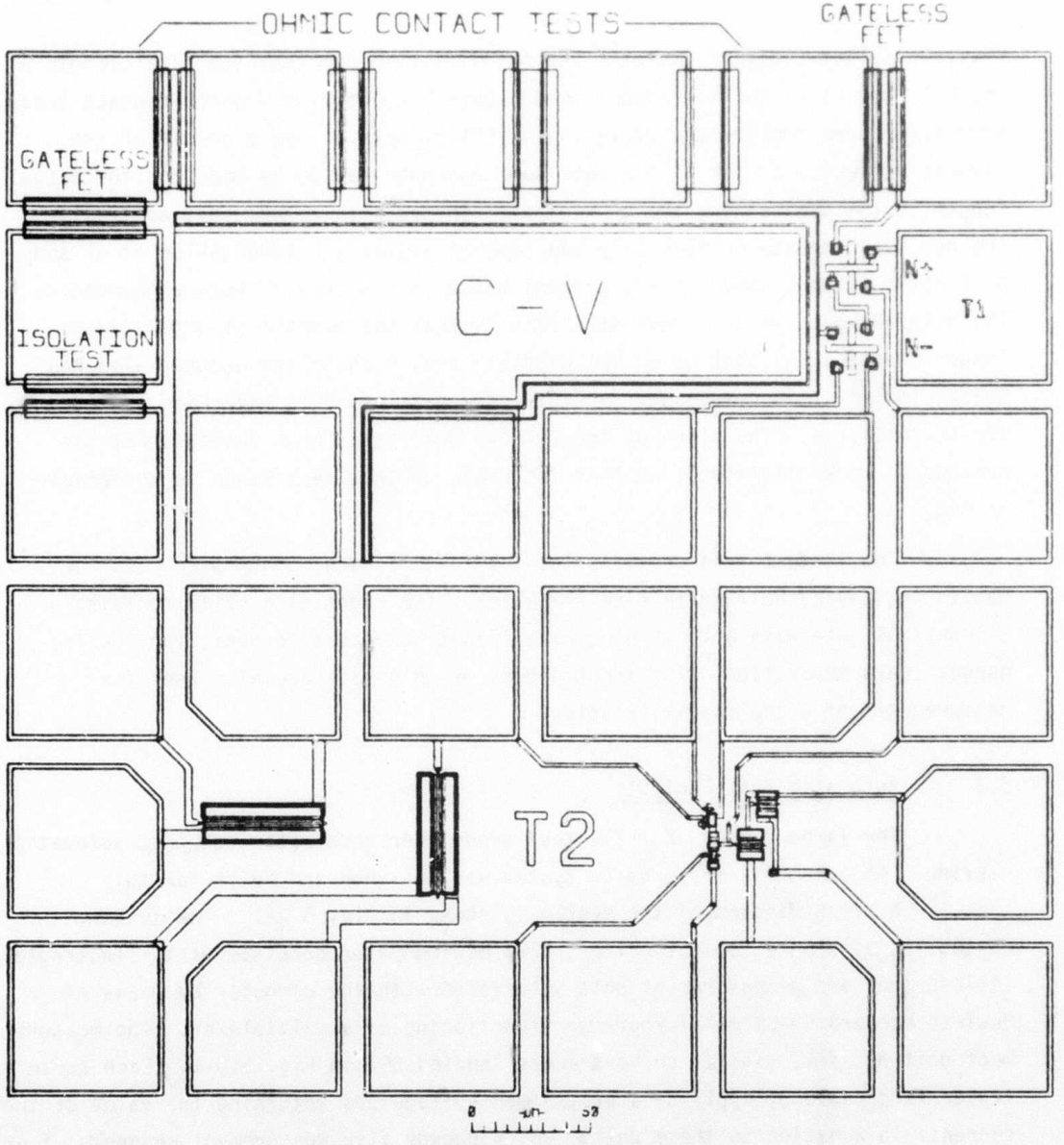

Fig. 5.2-1 Plot of the T1 and T2 test cells. The overall dimension is 440 × 440 μm.

This n^+ implant (sulfur) exhibits lateral diffusion, so that the final length of the FET channel is not well determined. Until recently, the ohmic contact test structures were implemented imitating an FET structure. As a result of the lateral diffusion of the n^+ implant, some estimate had to be made for the actual length of the gap between the n^+ regions. In order to remove this ambiguity, the new test structures have only one type of implant, a combination of n^- and n^+ forming not only the contact regions but also the channel between contacts. The only drawback of this test structure is that the overall structure is no longer identical to that of an FET without gate, because the channel also has the n^+ implant. To compensate for this, two gateless FETs have been provided in the T1 test area. The slope of the I-V characteristic of a gateless FET can provide a quick estimate of whether the ohmic contact resistance is acceptable or not.

The T2 test area contains two 1 μm gate length, 50 μm wide FETs for monitoring device uniformity over the wafer. The right side of T2 contains a 2-input NOR gate with all its electrical nodes connected to pads, for low frequency characterization. The input diodes of this gate are also used for measurements of diode characteristics.

5.3 Automatic Test Facility

The large number of T1/T2 test areas over each wafer requires automatic testing. An automatic measurement system was designed and built for this task.[28] A block diagram of the system is shown in Fig. 5.3-1. The system, controlled by a Data General Eclipse S230 minicomputer consists of an Electroglas 1034X prober and a measurement unit interfaced with the computer by means of Hewlett Packard 6940B multiprogrammer functioning as a multiplexer. The measurement unit has five digital curve tracers labeled DCT in Fig. 5.3-1. Each curve tracer is capable of applying a programmed voltage and returning the value of the current. In addition to these units, which occupy five measurement channels, four additional channels are used for a programmable current source, an A/D converter for floating voltage measurements, and a ground connection. The system is equipped with a computer controlled cross-point switch, made with Reed relays, capable of connecting any of 20 probe inputs to any of the 10 measurement channels.

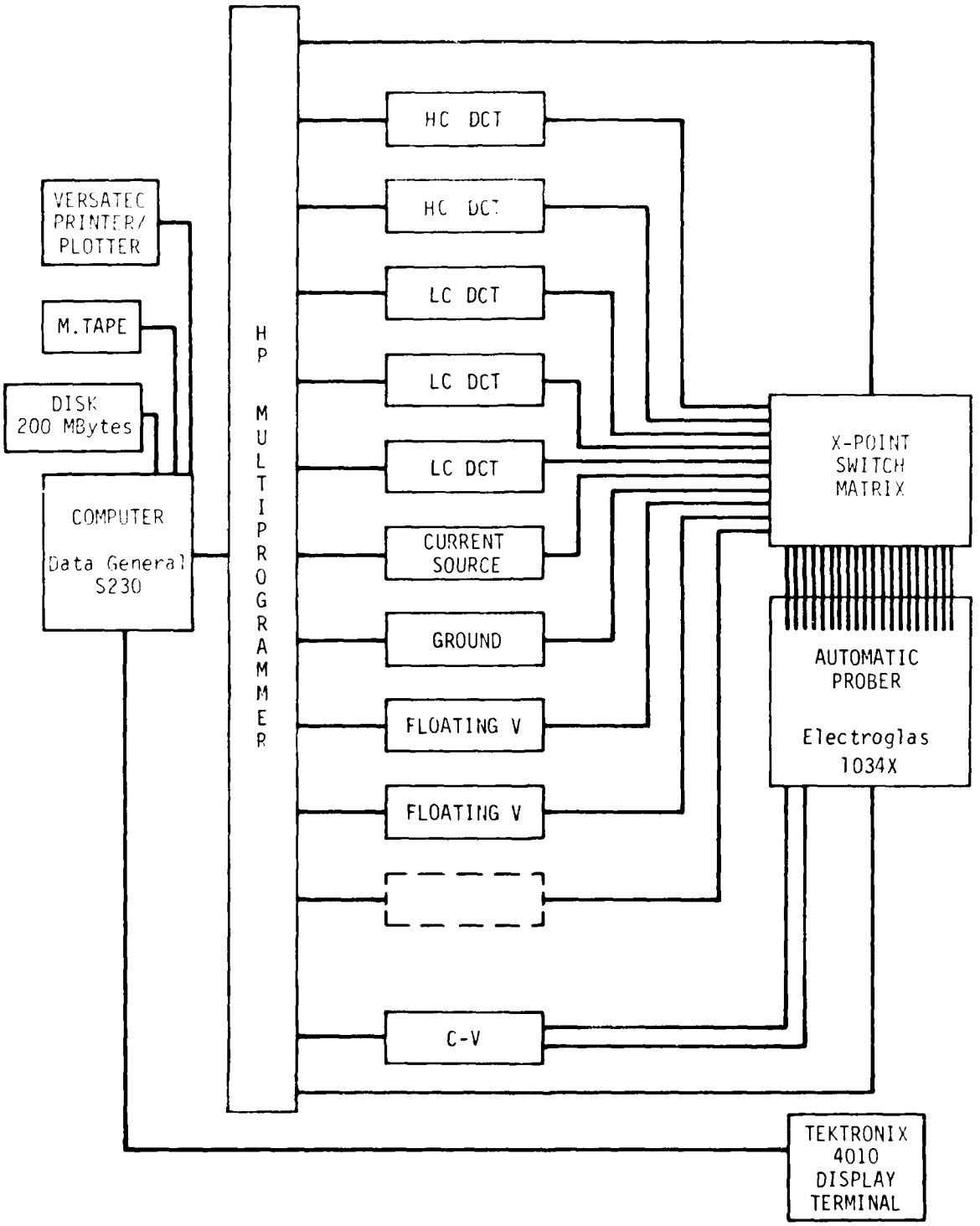

Fig. 5.3-1 Block diagram of the automatic test system.

The automatic test system has been programmed to acquire I-V characterisics of diodes and FETs, and to analyze these characteristics. The diodes are modeled as ideal diodes with a resistor in series. Least square fitting of the data yields the reverse saturation current, the ideality factor, and the series resistance. The analysis of the FET characteristics yields a number of parameters, the most important ones being the pinchoff voltage, the saturation current, the on-resistance, and the saturation voltage. The programs which perform FET and diode analysis also survey the characteristics for device failure, identifying failure modes.

C-V measurements are also performed by the automatic system. The capacitive component of an ac current through the diode is measured by a current amplifier followed by a lock-in amplifier. The computer controls the diode bias voltages and acquires the amplitude of the ac current. This is done through direct coaxial connections to the probe card avoiding the parasitic capacitance of the X-point matrix.

The results from device analysis are stored on disk files, and are normally examined by means of programs which provide graphic display of the results in the form of wafer maps and histograms. The data in the following section are good examples of such graphic display capability.

Work is under way for architectural improvements of the automatic test system. A microcomputer system with analog and digital I/O capability will replace the HP multiprogrammer (Fig. 5.3-1). The microcomputer will take care of all the data acquisition functions responding to a computer command, and it will temporarily store the data on its own disk. After a measurement is completed, the data will be transferred to the computer for final storage, analysis and display. This architecture will alleviate the demands on the computer, making it more efficient, while preventing the measurements from being slowed down by other tasks competing for computer resources.

5.4 Statistical Results

Figure 5.4-1 shows a wafer map and a histogram for the turn-on voltage of the logic diode.[28] The turn-on voltage, labeled V@.15MA in the figure, is

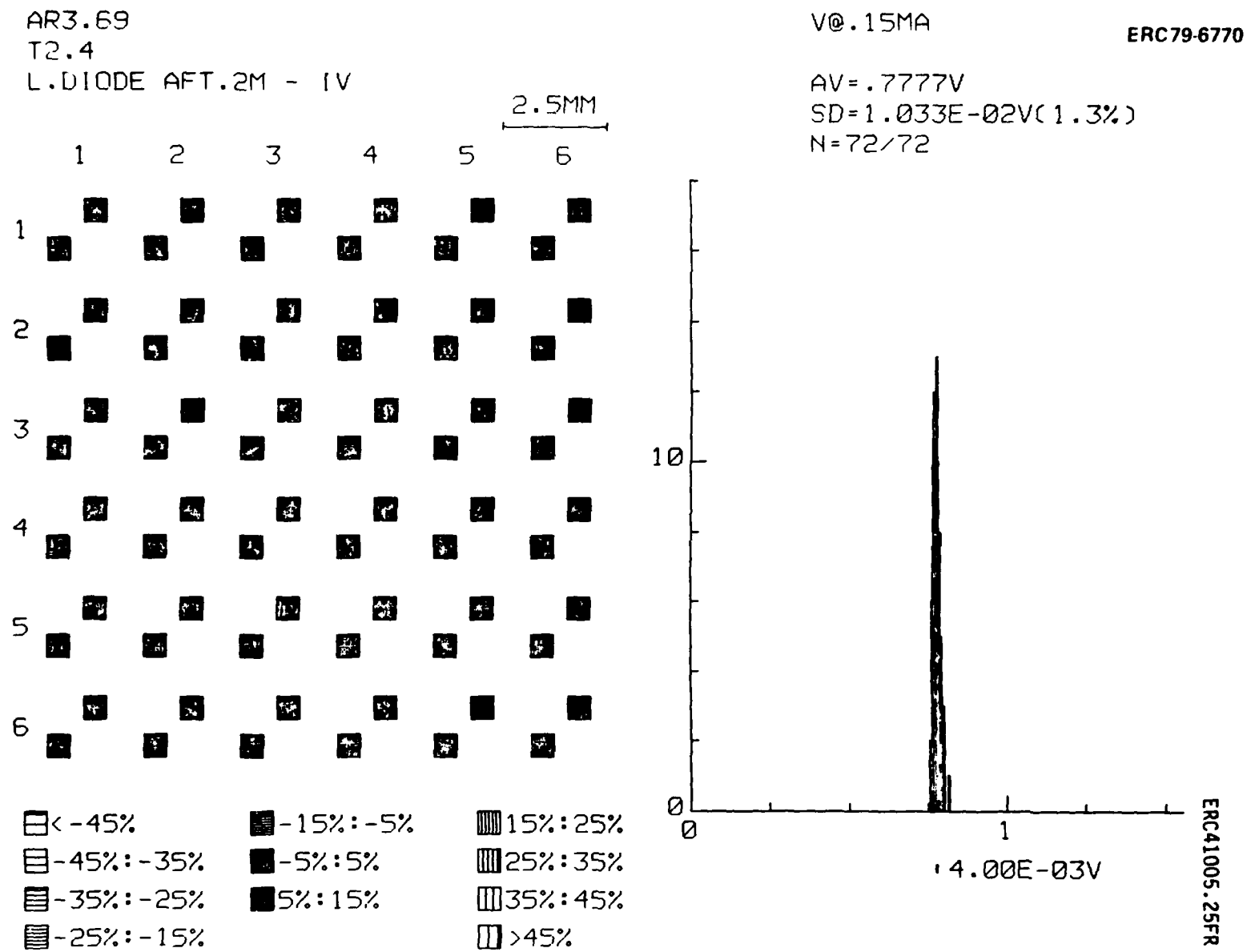

Fig. 5.4-1 Map and histogram for the turn-on voltage of the logic diodes in the T2 test area of the wafer. The turn-on voltage V @ .15 MA is defined as the voltage required to sustain a forward current of 0.15 mA.

the voltage required to sustain a 0.15 mA current, which is the typical forward current for logic diodes in standard SDFL gates. Figure 5.4-1 is also an example of graphic display of device parameters by the automatic test system. The right side contains a histogram with printed values of the average and standard deviation of the parameter. The left side shows a map of the wafer (compare with Fig. 5.0-1) indicating, for each device, the amount of deviation of the parameter (turn-on voltage in this case) from its average value. The magnitude of the variation is keyed by the type of cross hatching according to the scale below the map. Such maps are useful for identifying variation trends across the wafer. In this example, the parameter is very uniform over the wafer. Its standard deviation is only 10 mV, 1.3% of its average value. Such excellent uniformity indicates good Schottky barriers, very uniform lithography (the diode area is ony 1 x 2 μm) and good ohmic contacts.

A map and a histogram for the pinchoff voltage of FETs (50 μm width, 1 μm gate length) is shown in Fig. 5.4-2. The uniformity of this wafer is among the best observed, with a standard deviation of pinchoff voltage equal to 48 mV. More typical statistical results are shown in Fig. 5.4-3, where for the sake of brevity, four statistical displays similar to the ones in Figs. 5.4-1 and 5.4-2 were condensed into one figure containing the histograms for the four principal parameters of the FETs. These parameters are the pinchoff voltage VP, the saturation current IDSS, the on-resistance RON, and the saturation voltage VSAT. The uniformity of device parameters displayed in Fig. 5.4-3 is still excellent. The standard deviations of the parameters range between 4.4% and 7.5% of their average values. The standard deviation of pinchoff voltage, 7.5% of the average (which is 1.24V) represents 94 mV.

The data presented so far provide insight into the uniformity of FET and diode parameters across a wafer. However, the test devices are relatively far apart from each other (~ 2 mm), much farther than devices within a circuit. Uniformity over a small area of the wafer was evaluated with the aid of the FET array test pattern located in the PM chip. The FET array consists of 81 (9 x 9) devices, 20 μm wide, 1 μm gate length, spaced 30 μm center to center in each direction. On mask set AR5, two such arrays, having 81 FETs each, were placed

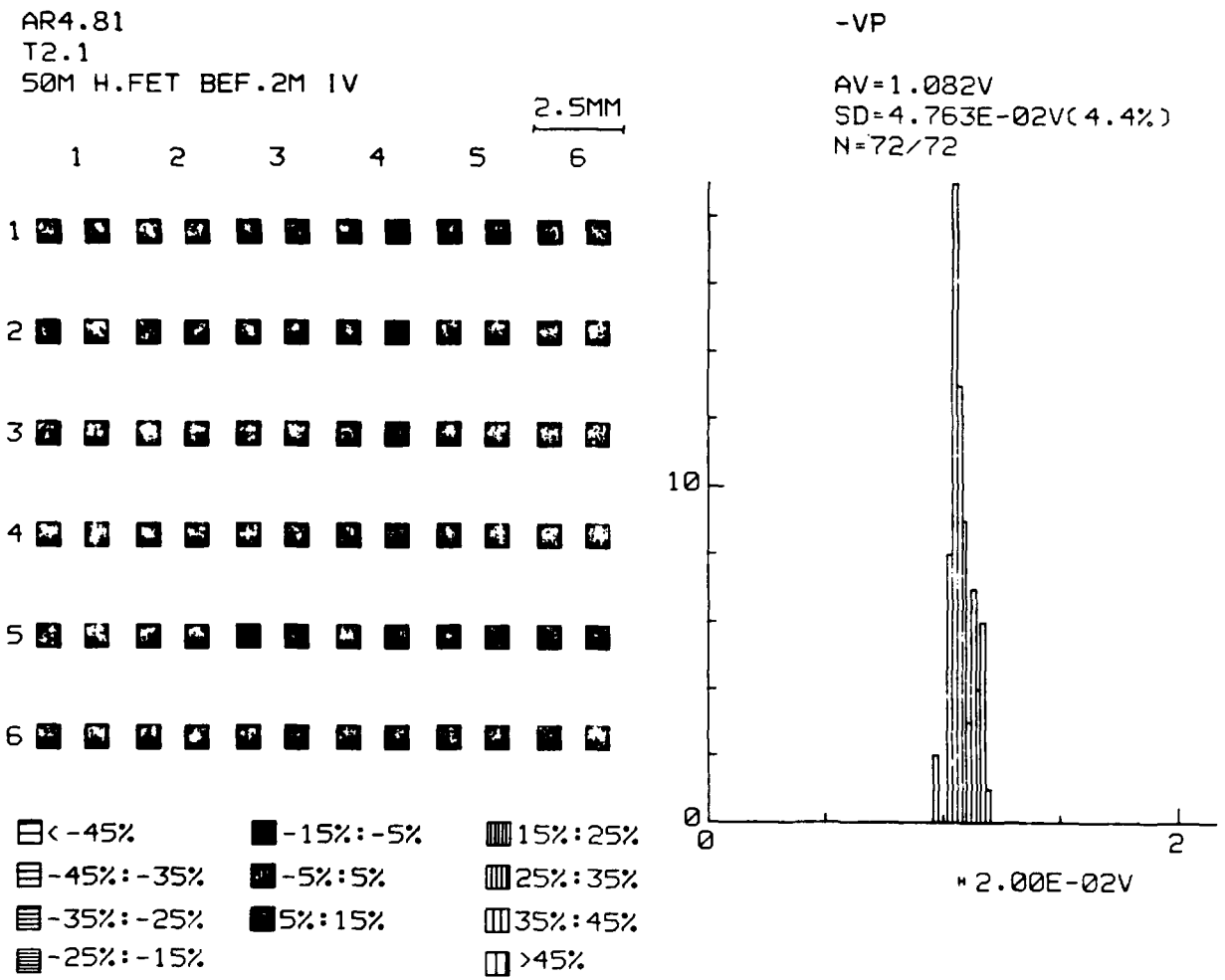

Fig. 5.4-2 Map and histogram for the pinchoff voltage (V_p) of the test FET (50 μm wided, 1 μm gate length) in the test areas T2 of an IC wafer. The very low standard deviation of V_p across this wafer, 48 mV, represents the best values to date.

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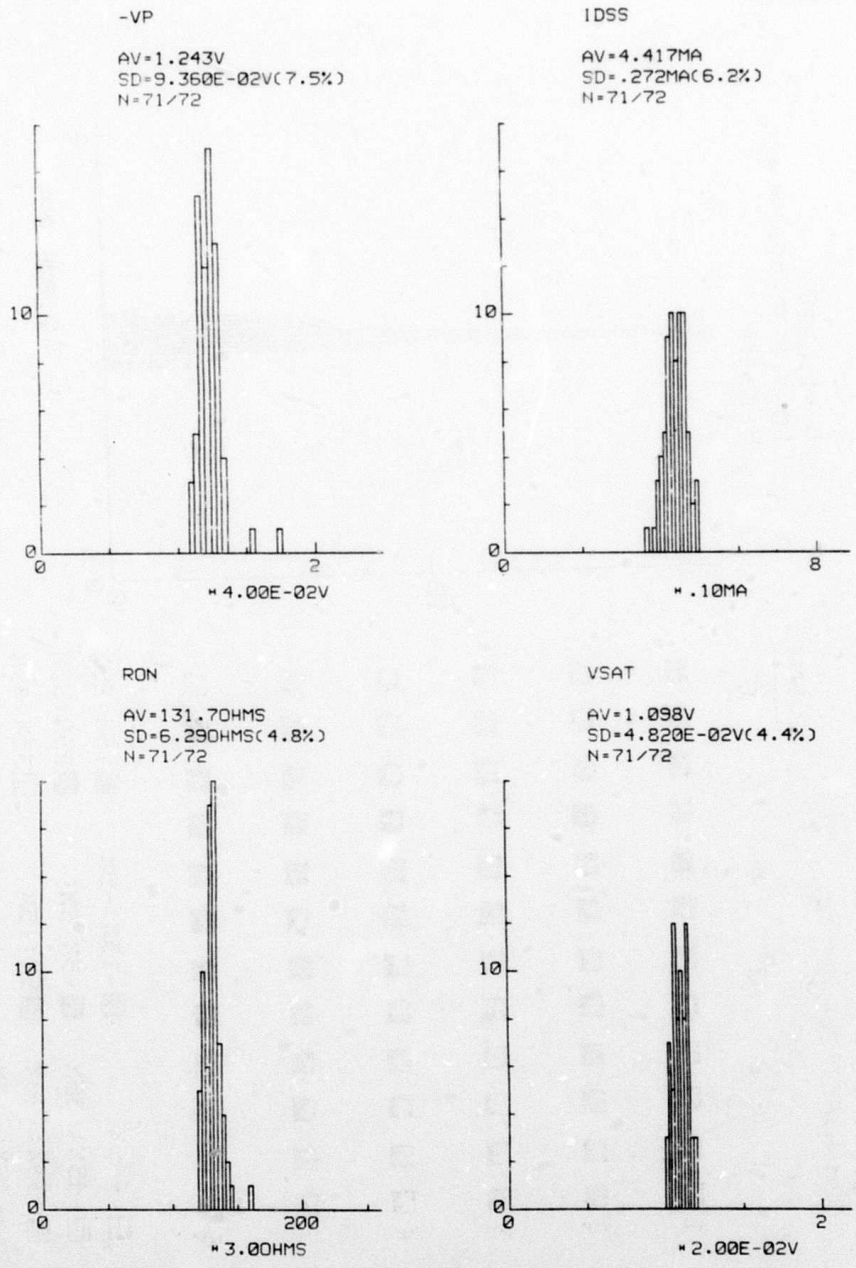

Fig. 5.4-3 Histogram of pinchoff voltage V_p, saturatin current I_{dss}, on resistance, RON and saturation current VSAT for the FETs (50 μm wide, 1 μm gate) located in the T2 test areas. The data are from the same wafer on which the diodes were mapped (Fig. 3.4-9).

next to each other to form a virtual 162 FET array. The FET array measurements were made using the automatic test system described above. The cross point relay matrix (Fig. 5.3-1) handled the switching of connections required to access each device.

Figure 5.4-4 shows a histogram of pinchoff voltages and a histogram of saturation currents for one of the 182 FET arrays. The standard deviation of pinchoff voltage over the array is very low, only 17 mV (1.2% of the average value). This is a remarkable improvement with respect to the wafer standard deviation which was 67 mV. The lower standard deviation of pinchoff voltage indicates better uniformity of carrier concentration profiles over a short range.

The FET array data discussed so far correspond to a wafer which exhibits excellent long and short range uniformity. On average wafers with standard deviations of pinchoff voltage on the order of 80 to 90 mV over the whole wafer, the standard deviation of pinchoff voltage for the FET array is typically on the order of 30 mV. Poor wafers characterized by large variations of device parameters over the long range exhibit more dramatic improvements over the short range. Even such wafers have some test arrays with standard deviations of pinchoff voltage of ~ 30 to 40 mV.

To complement the device statistics, a histogram of gate threshold voltages is shown in Fig. 5.4-5. The data were taken from the same wafer from which the data in Figs. 5.4-1 and 5.4-3 were taken. The average threshold voltage of 1.314 V and its 57 mV (4.3% of the average) standard deviation are consistent with the statistical data from single devices.

Establishing a relationship of the parameter variations to circuit yields is a difficult task in that the fundamental yield-limiting mechanisms in these GaAs ICs have not been determined, and certainly some yield limitation will result from material or processing defects unrelated to the statistical variation of device parameters. However, the observed statistical parameter variations of the devices, analyzed in terms of their influence on the static or dynamic circuit operation, can provide an upper limit estimate for the anticipated circuit yields. Conversely, this same information can be used to indicate

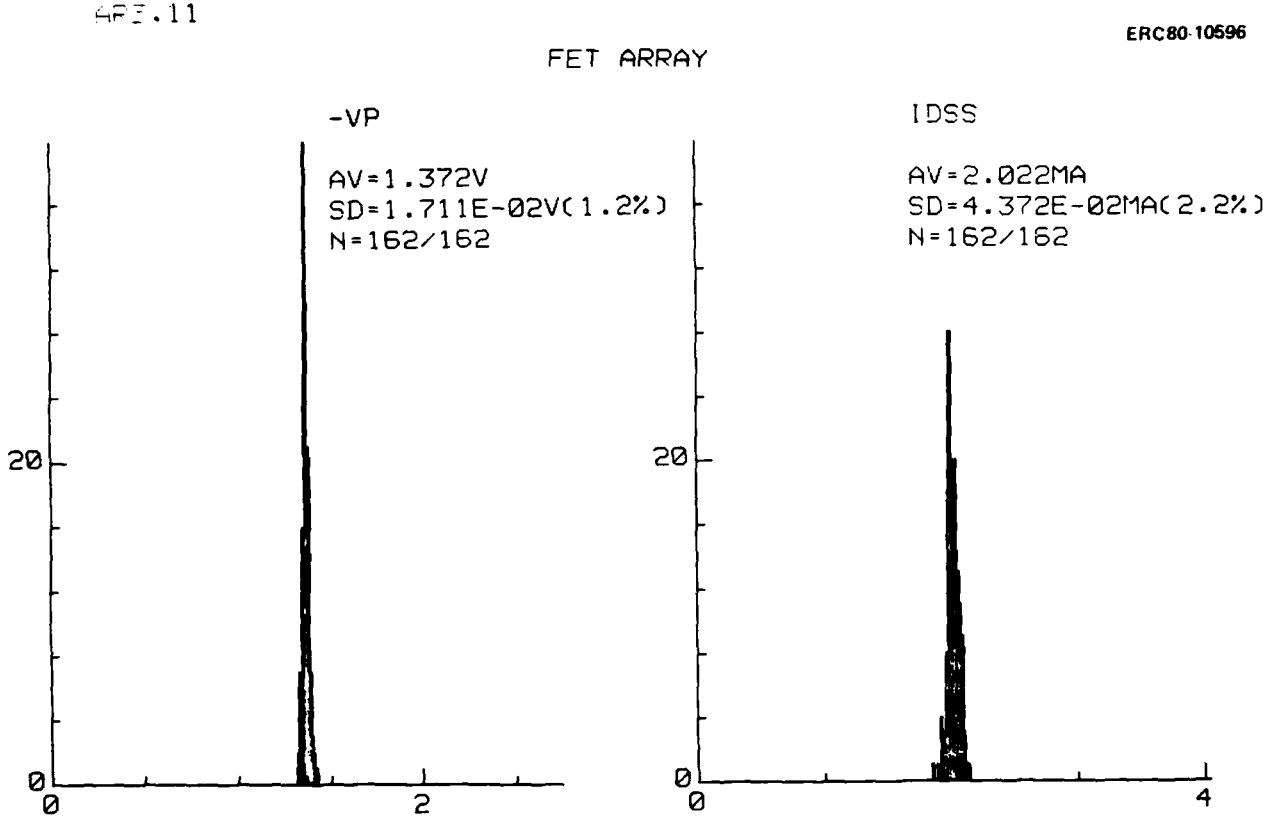

Fig. 5.4-4 Histogram of pinchoff voltages (-VP) and saturation current (IDSS) for an array of 162 50 μm wide, 1 μm gate length test FET spread over an area of 300 × 750 μm.

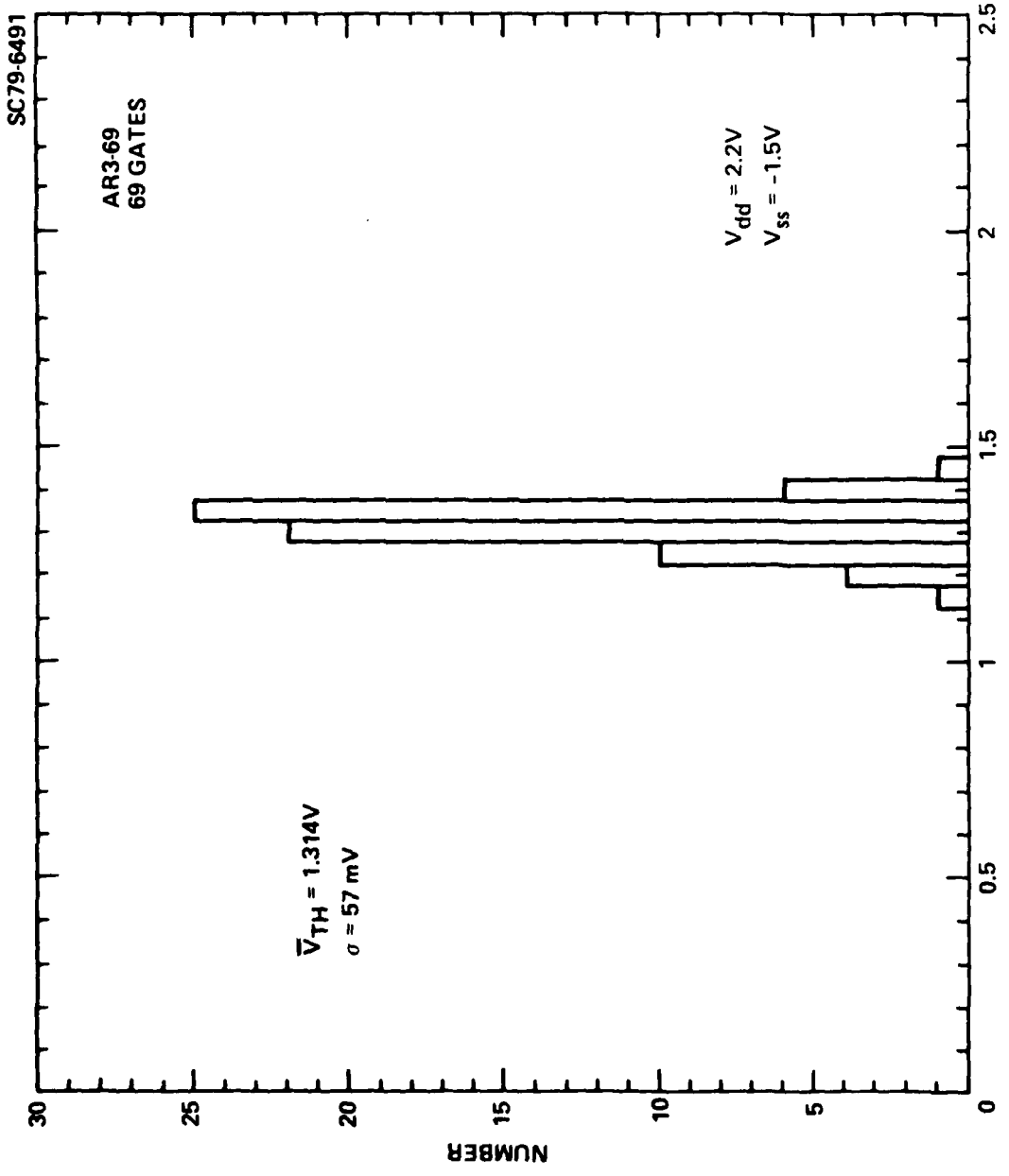

Fig. 5.4-5 Histogram of gate threshold voltage for the test gate in the T2 test area. The data are from the same wafer from which previous diode and FET data were obtained (Figs. 3.4-9, 3.4-11 and 3.4-12).

appropriate design tradeoffs to optimize yield with minimum sacrifice in performance in circuits of various complexities. At the simplest level, the effect of parameter variations on circuit static yield may be considered through the probability of exceeding either the input voltage noise margin of gates or the output current noise margin. In the depletion-mode SDFL logic circuits, the typical voltage noise margins are of the order of 0.6 V or more on either a "high" or "low." In comparison to the observed $\sigma_{V_p} < 80$ mV (and sometimes lower) wafer uniformities (let alone the $\sigma_{V_p} < 30$ mV short range uniformities), the statistical probability of exceeding the voltage noise margin is negligible. This is a consequence, of course, of the fact that the logic voltage swings and noise margins have been kept fairly large in the SDFL circuit designs in order to cope with the significant switching transient-induced ("hash") noise levels that are commonly present in very high speed digital circuits and systems.

The current noise margins, or relationship between the current drive capability of a gate and the input current requirements of its fan-out of loading gates, is a different issue. In general, optimum switching speed performance is obtained when the source drive capabilities and loading gate input current requirements are closely matched. This is always the case for transient currents in dynamic measurements on FET logic circuits but it is even more obvious in SDFL where this is also reflected in a static fan-out limitation because of the dc input current requirements of the gates. The static fan-out, and hence the current noise margin, may be increased in the SDFL circuits by increasing the ratio of the output pullup to the input pulldown active load current ratio (by adjusting device widths). On the other hand, increasing this ratio much beyond that required to meet the particular fan-out loading conditions for the gate involves some sacrifice in switching speed. For this reason, most of the SDFL circuits are fabricated with a current noise margin of only about 30%. With long-range standard deviations in device saturation currents, $\sigma_{I_{dss}}$, in the 6% to 8% range, little influence on yield would be observed, even for >1000 gate LSI circuits. If $\sigma_{I_{dss}} = 10\%$, significant yield reductions (to about 26% on 1000 gate circuits) would be expected, so that it would be necessary to raise the current noise margin slightly. Here the IC designer can draw valuable information from the statistical data.

The data accumulated also provide a good data base for process statistics. As an example, Fig. 5.4-6 shows a plot of average saturation current vs average pinchoff voltage of the 1 μm gate length, 50 μm wide test FETs in T2 for a very large number of processed wafers. Each point in the figure corresponds to one wafer. The pinchoff voltage ranges between 0.45 V(for very low power circuits) and 2.0 V (for high speed) with the largest number of wafers in the 0.7 - 1.0 V interval. The plot shows strong correlation between saturation current and pinchoff voltage, with the points falling on a nearly parabolic curve. The strong correlation is due to the reproducibility of the process observed in spite of the long time (over two years) over which the data were taken. The result of a least square fit is printed on the upper left corner of Fig. 5.4-6. This curve provides valuable information to the circuit designer.

The average pinchoff voltage of test FETs displayed in Fig. 5.4-6 are plotted again in Fig. 5.4-7, but here they are displayed as a function of time. Each data point in the figure represents the average pinchoff voltage for one wafer. Although certain trends and variations as a function of time are the results of intentional changes in implantation doses, the figure shows smaller fluctuations as time progresses. This improvement is due to better process control, and also, to some extent, to narrowing the range of experimentation with pinchoff voltages as a result of learning from circuit testing.

In Fig. 5.4-8 the standard deviations of pinchoff voltage corresponding to the same wafers used for Fig. 5.4-7 are displayed as a function of time. Again, each data point corresponds to one wafer. The figure shows that the density of points representing standard deviations lower than 100 mV has increased with time. This is the result of better process control. A standard deviation of pinchoff voltage of 100 mV is considered the limit below which a wafer is rated as having "excellent" uniformity.

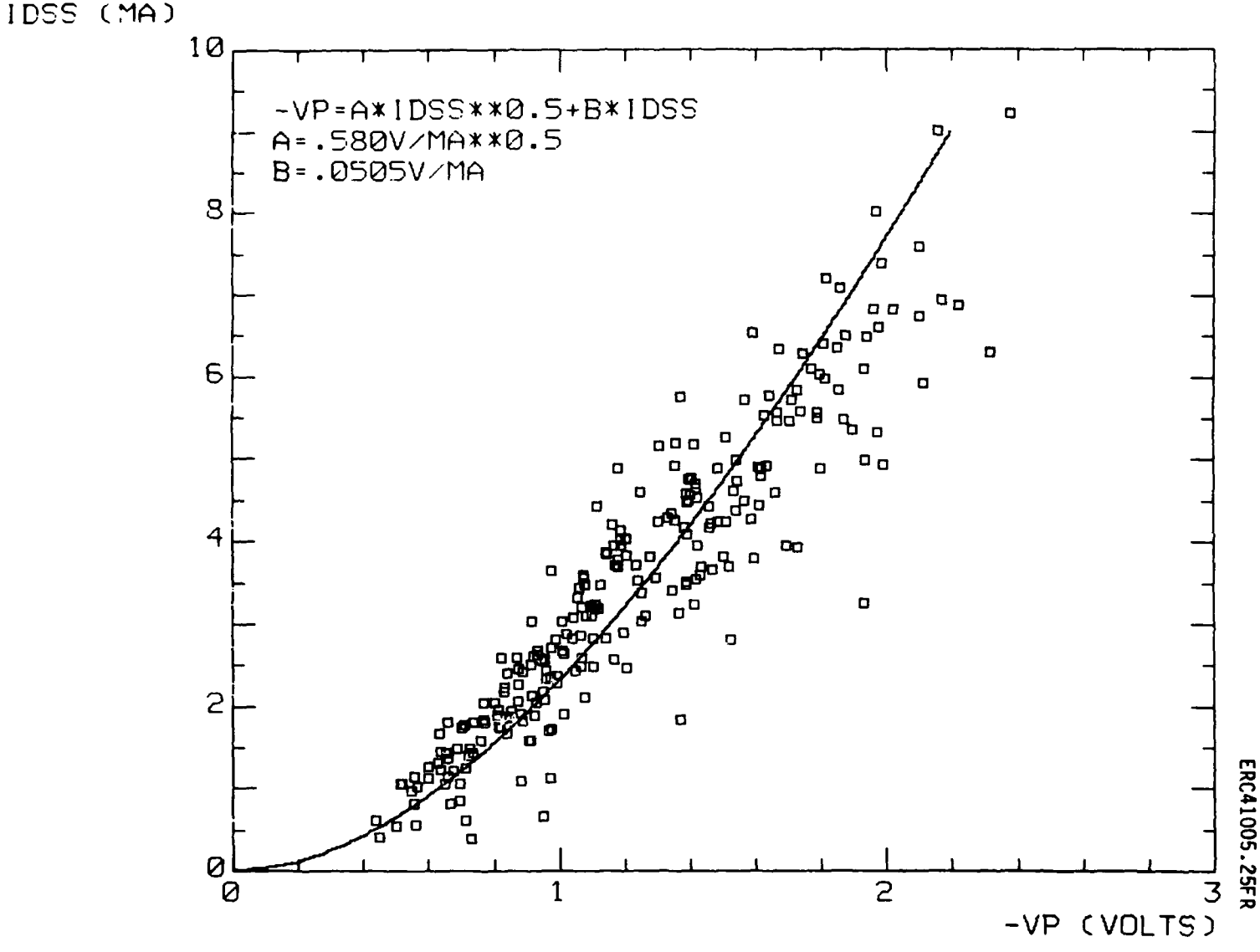

Fig. 5.4-6 Wafer average of saturation current vs average pinchoff voltage for the 1 μm gate length, 50 μm wide test FETs in the T2 test area. Each point corresponds to one wafer. The result of a least square fit is printed on the upper left corner.

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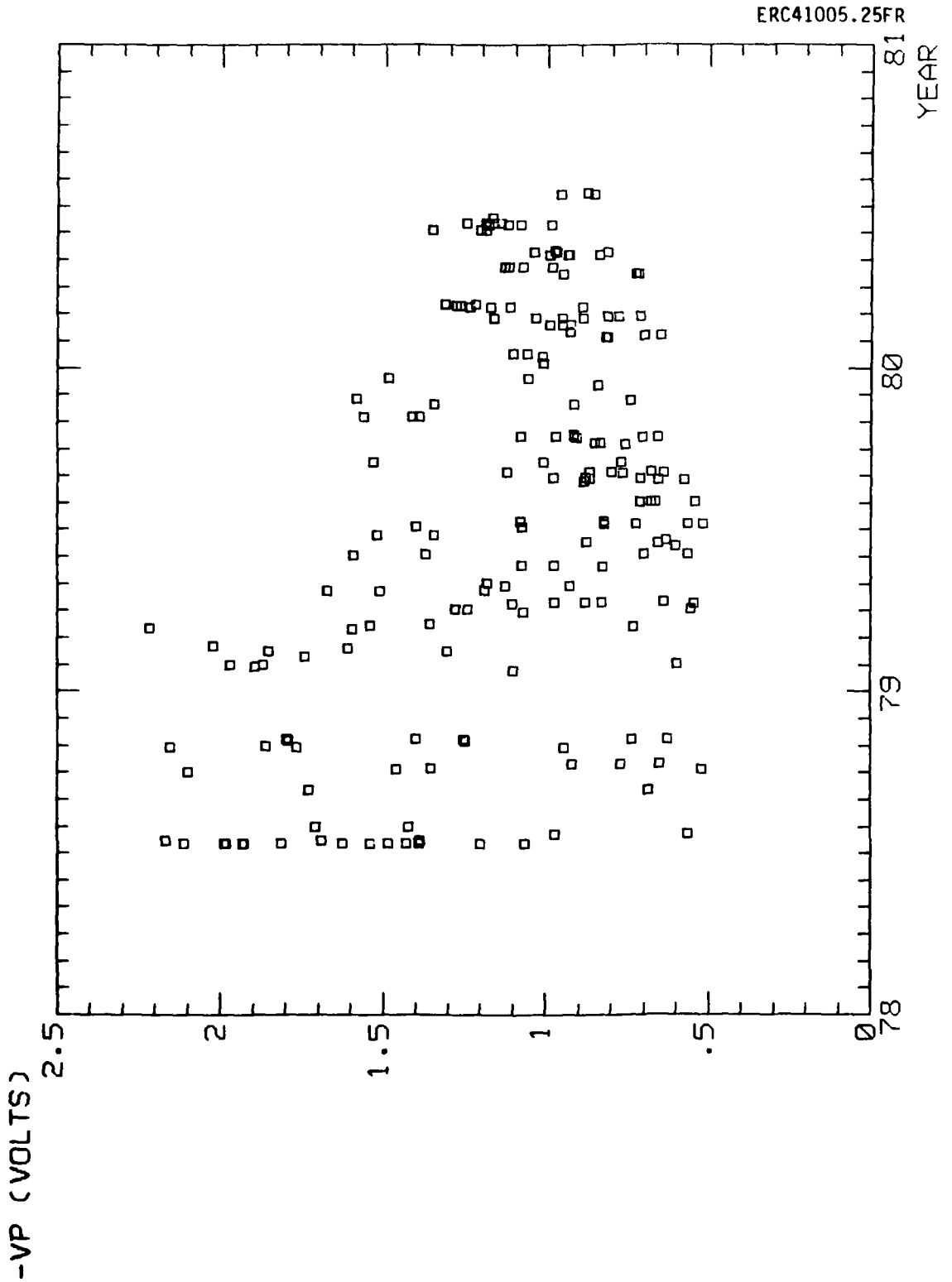


Fig. 5.4-7 Average pinchoff voltage for the 1 μm gate length, 50 μm wide test FETs in test areas T2. Each data point corresponds to one process wafer.

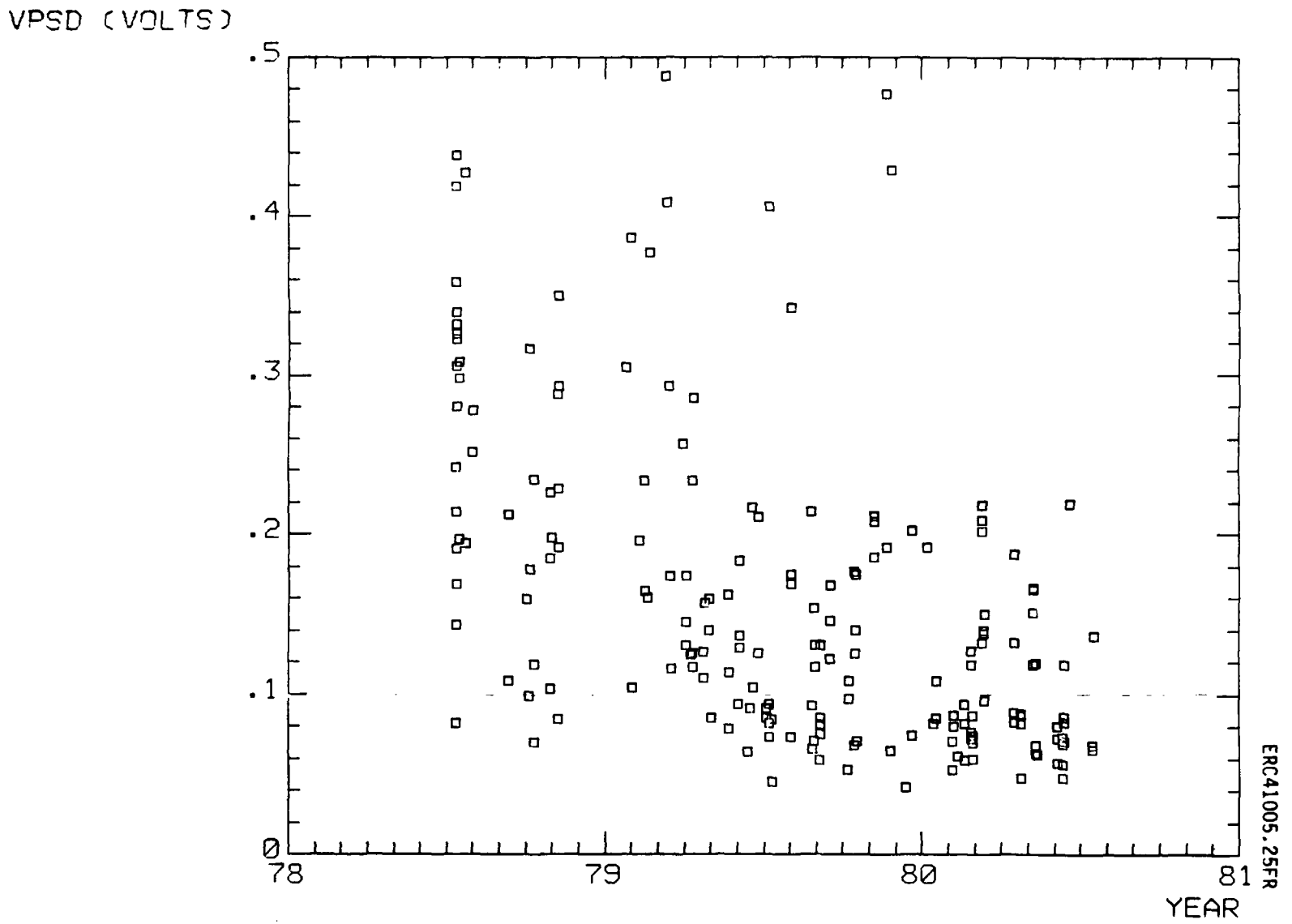


Fig. 5.4-8 Standard deviation of pinchoff voltage for the 1 μm gate length, 50 μm wide FETs in test areas T2. Each data point corresponds to one wafer.

6.0 SDFL CIRCUIT DESIGN AND PERFORMANCE

The Schottky Diode FET Logic gate has been designed to take full advantage of the flexibility provided by the planar fabrication process. These logic gates require moderate to low powers (0.2 to 2 mW/gate), are capable of very high densities (up to $10^5/cm^2$) and provide very high speed (as low as 62 ps/gate for a 10 μm NOR gate). The SDFL NOR gate has provided a building block which was used to design many MSI and, more recently, LSI GaAs IC's. In the following sections, the design and evaluation of such circuits is presented. In Section 6.1, the SDFL gate design is presented along with ring oscillator dynamic performance evaluations. Section 6.2 describes the circuit and device modeling efforts which were necessary for the design of more complex MSI and LSI circuits. The contributions made by the Cornell University MESFET modeling effort are discussed in this section. Sections 6.3 and 6.4 describe the design and complete functions and high speed evaluation of MSI/LSI demonstration circuits fabricated for this program. Samples of divide by 8 circuits were packaged and delivered as discussed in Section 6.5. Section 6.6 describes the temperature range testing and radiation hardness characterization performed on the planar SDFL circuits.

6.1 Schottky Diode FET Logic Gate Design

The basic building block for any high speed digital circuit is the logic gate. Since very high densities of logic gates per chip are desired for LSI applications, the basic gate must be designed to minimize wafer area and power dissipation as well as maintaining low propagation delay. The planar, multiple localized implant approach used in this project allows fabrication of both optimized Schottky barrier switching diodes and FETs on the same circuit. Therefore, a circuit approach using small area (1 μm x 2 μm), high speed GaAs Schottky barrier switching diodes has been developed to provide most logic functions, with GaAs Schottky gate FETs used for inversion and gain, as shown in Fig. 6.1-1. This Schottky diode-FET logic (SFDL) approach allows major savings of chip area compared to the previous approaches in which FETs, either in series (NAND) or parallel (NOR) have been used as the logic elements.[29] For example, a

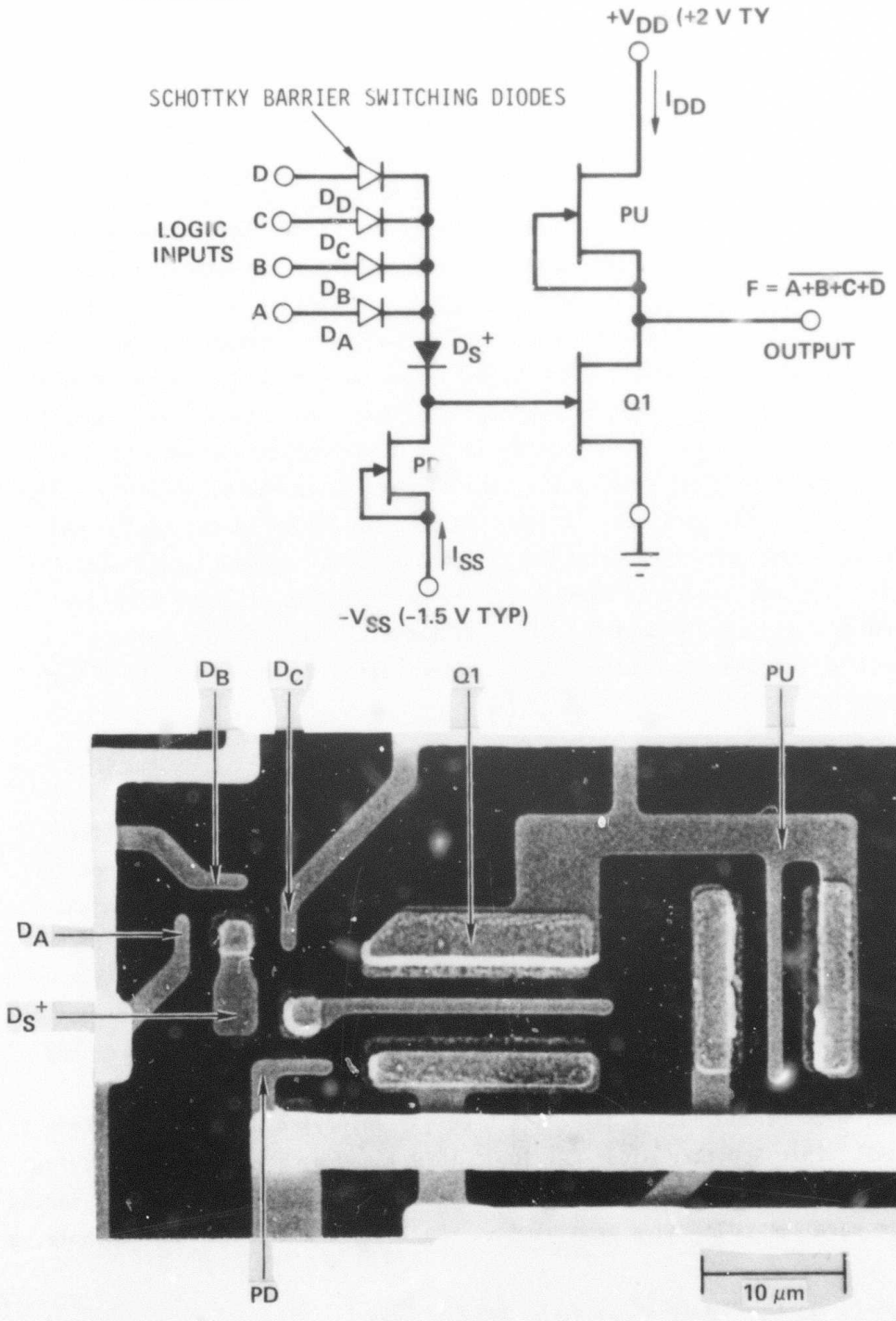


Fig. 6.1-1 A schematic and SEM micrograph of a SDFL NOR gate.

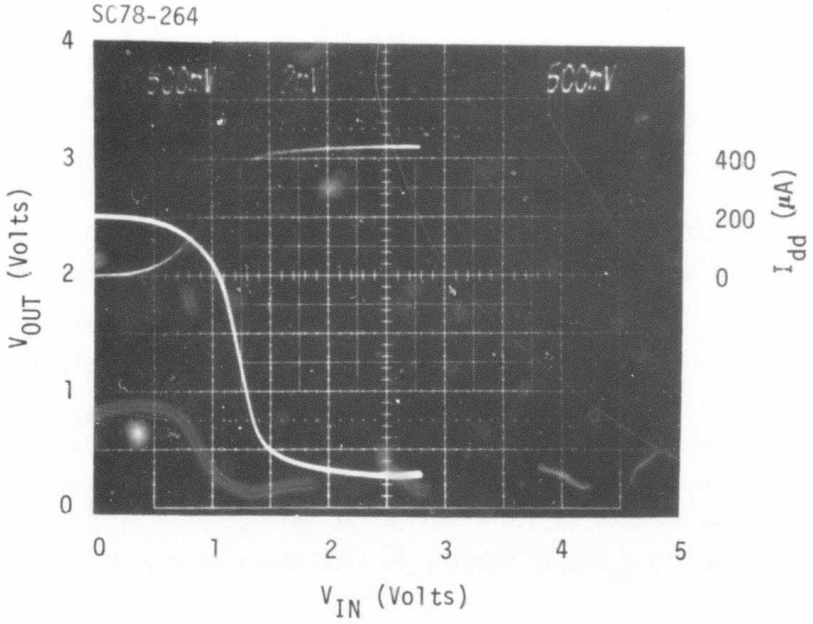
4-input NOR gate in FET logic (enhancement or depletion) would have as a minimum 4 switching FETs (each input as a FET gate) plus an active load pullup (or resistor load). As shown in Fig. 6.1-1, the SDFL approach requires only the single FET with its load, and four very small switching diodes. In addition to performing the "OR" logic function, these input diodes also provide some (or all) of the level shifting required between drain and gate in depletion-mode logic. Although significant savings in area results because of the much smaller size of a Schottky barrier diode as compared to a FET, additional area is saved because the diode is a two-terminal device, so that the many overcrossings associated with the use of 3-terminal logic elements are avoided. As a result, gate areas as low as 600 μm^2 have been possible for NOR gates with 5 μm unit FET widths.

Since most of the gate power dissipation, even in the SDFL approach, is in the GaAs FET or pullup (PU) active load, devices with low pinchoff voltages (0.75 - 1.0 V) are used to minimize drain current and reduce the required logic voltage swing.

Figure 6.1-2 shows the low frequency input-output transfer characteristic for a 10 μm NOR gate. This gate is identical to the one shown in Fig. 6.1-1. For this measurement one of the two inputs was left open, the equivalent to a "low" logic input, so that the gate was operating like an inverter. The threshold voltage is 1.5 V and the ac gain at threshold is approximately 4. The positive supply current is also shown in Fig. 6.1-2.

High Speed Performance of the NOR Gate - Ring Oscillator Results

The ring oscillator circuit provides a convenient method for evaluation of propagation delay τ_d, speed-power product, $PD\tau_d$, and power dissipation. A chain of an odd number of inverting logic gates is connected in a ring, so that the measured frequency of oscillation is related to the intrinsic gate propagation delay by $f = 1/(2N\tau_d)$, where N is the number of gates. Oscillators with gate fanouts of 1 or 2 are generally used. The number of stages is chosen so that the oscillation frequency will be low enough that accurate measurement equipment is available.



V_{dd} = 2.5V
V_{ss} = -2.0V

Fig. 6.1-2 Low-frequency input-output transfer characteristic for a 10 μm NOR gate. The larger curve is the output voltage, while the smaller curve near center is the positive supply current.

Figure 6.1-3 presents a schematic diagram and photograph of a 10 μm, NOR gate implemented, 9-stage SDFL ring oscillator. Two of the gates at the corners of the ring oscillator loop have two inputs, one of which can be utilized for gating ring oscillator oscillations with a lower frequency pulse to verify that meaningful logic swings are being achieved.

The output for high speed measurements is obtained through a capacitively coupled output buffer amplifier. This consists of a Darlington 1 μm long × 10 μm wide source follower driving a 1 × 55 μm output pad driver. This permits driving a 50 Ω load without significantly changing the transfer characteristics of any ring oscillator gates through external loading. The output stage is dc isolated from the ring oscillator so that a separate power supply can be used. Thus, the power dissipation of the buffer amplifier does not affect the accurate mesurement of dynamic switching energy.

A summary of high speed test data obtained from ring oscillator measurements is presented in Table 6.1-1. These circuits were composed of 5, 10 and 20 μm SDFL NOR gates, and 3 μm SDFL inverters. As seen in the table, the propagation delay and dynamic switching energy of the gates is dependent on the width of the FET channel. In general, gates composed of smaller FETs have longer propagation delays due to the reduced channel currents since the drain source current scales in direct proportion to channel width. Power dissipation is, of course, reduced by the use of smaller FETs, a technique which can be used to minimize power dissipation in a complex circuit when loading is small or speed is not extremely critical. The 10 μm ring oscillators are significantly faster, because many more wafers have been characterized with this size RO than any of the other sizes, and this data represents the fastest results obtained.

It should be noted that while the gate loading in these ring oscillators is one SDFL NOR gate, the propagation delay results would not be expected to be degraded very much by heavier fanout loadings (as would be expected for direct coupled FET logic like in NMOS or CMOS). The reason for this is that in the SDFL logic configuration, the gate turn-off current for the switching FET is not provided by the preceding FET drain current, but rather by the current of the much smaller pulldown (PD) to $-V_{SS}$, since the previous FET drain is isolated

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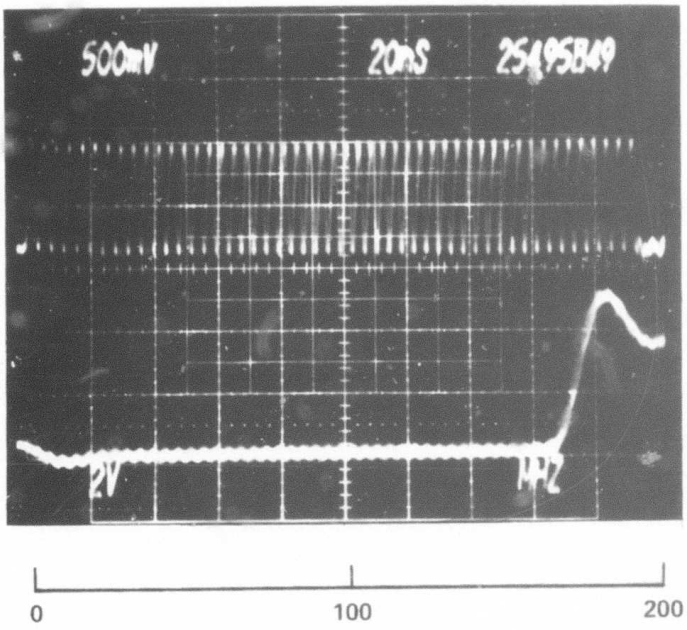

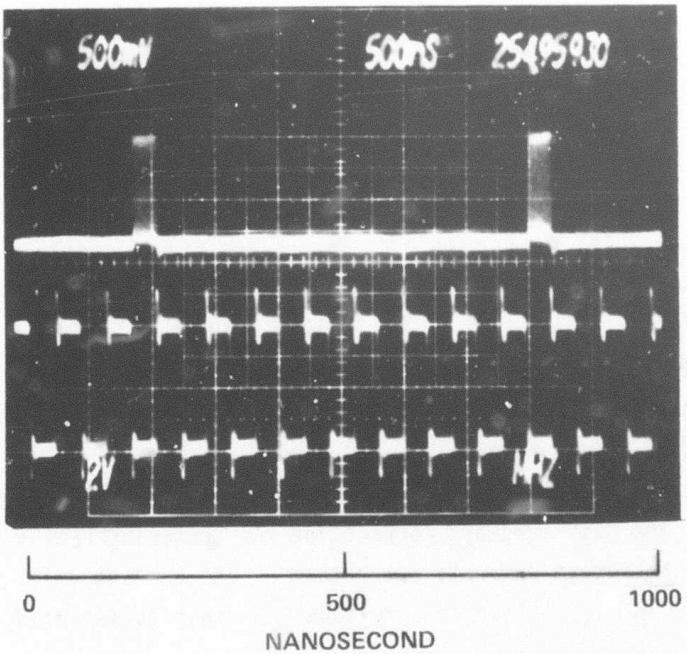

Fig. 6.1-3 Schematic diagram and micrograph of 10 μm. 9-stage ring oscillator.

Table 6.1-1

SDFL NOR Gate Ring Oscillator Performance

FET Width	τ_d (ps)	P_D (mw/gate)	$P_D\tau_d$ (fJ)
3 μm	136	0.118	16
5 μm	110.7	0.372	41
10 μm	62	0.865	65
	120	0.33	40
20 μm	75	2.3	170

by the switching diode (see Fig. 6.1-1). Hence, in effect, a fanout of 2 to 3 is built into the SDFL logic gate itself, so that the propagation delay should be only weakly dependent on fanout loading. Further, since the switching Schottky diode capacitance is very small, (~ 2fF for a 1 μm × 2 μm diode) the propagation delay should vary very little with the fan-in of the SDFL gates (number of gate inputs connected). In the ring oscillators measured, either one of two input SDFL NOR gates were used.

Figure 6.1-4 presents a comparison of speed/power performance measured on GaAs IC ring oscillators representing a broad range of circuit design approaches. Among depletion-mode circuits, the L_g = 1 μm SDFL design has achieved lower speed-power products ($P_D\tau_d$ = 16 fJ with τ_d = 136 ps for W = 3 μm inverters) while achieving similar speeds. In fact, in the W = 10 μm range practical for LSI, the results for L_g = 1 μm SDFL NOR gate ring oscillators (τ_D = 62 ps at $P_D\tau_d$ = 68 fJ) are in fact better than the results published for W = 10 μm L_g = 0.5 μm BFL inverters operating at over five times higher power levels.[30] SDFL inverters would be expected to be even faster than these NOR gates. The gate areas in this SDFL approach are excellent, with densities in excess of 10^5 gates/cm^2 demonstrated. In addition, speeds and speed-power products consistent with ring oscillator measurement have been maintained in planar LSI ICs with up to 260 gates (see Section 6.4).

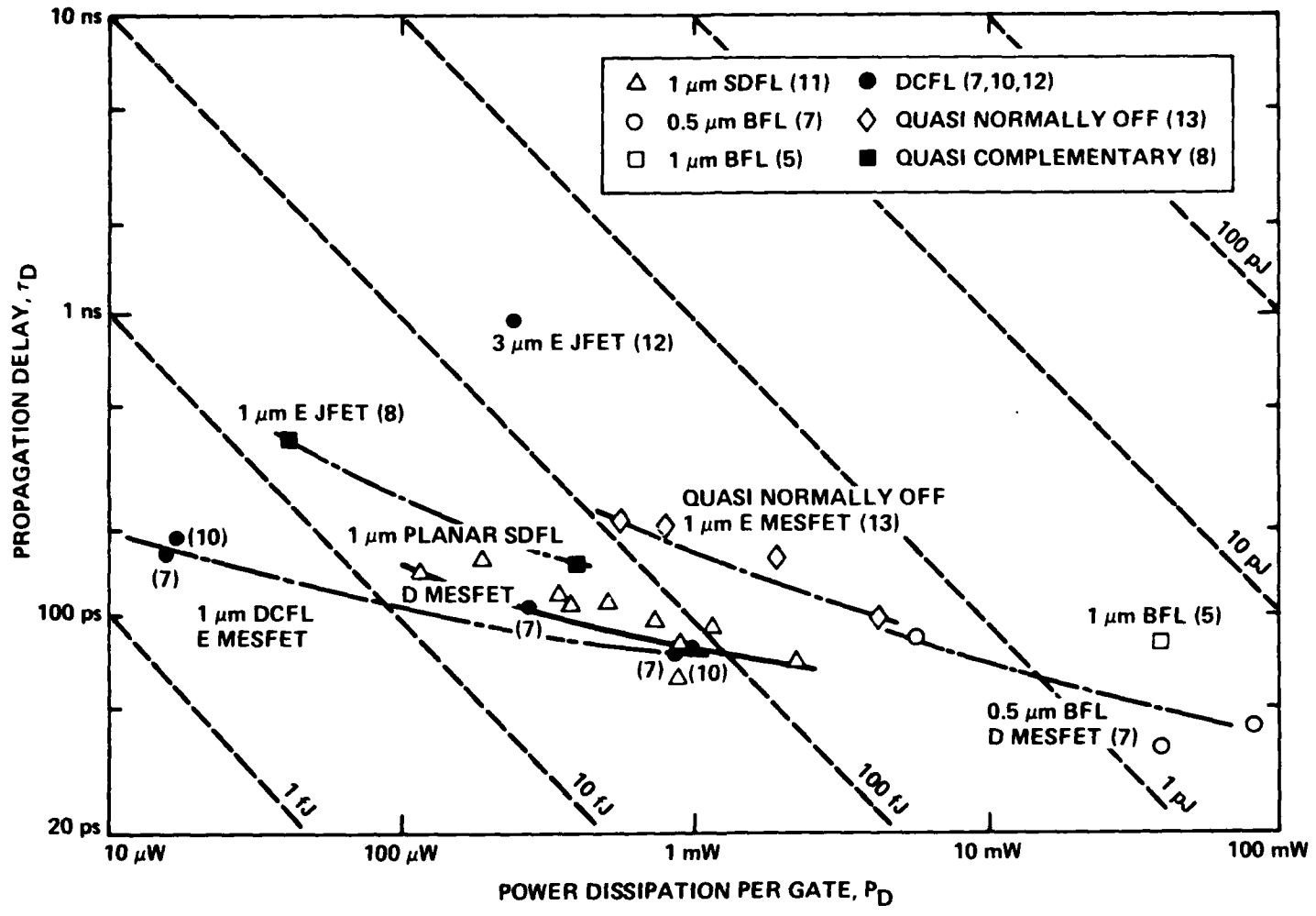

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Fig. 6.1-4 Speed-power performance comparisons of GaAs ring oscillators.

A logic gate circuit design must also be capable of extension to two or more levels of logic per gate delay in order to realize the highest speed, to minimize chip area and power dissipation for a given IC logic technology. (A logic level consists of one (N)AND or (N)OR operation of arbitrary width.) Multilevel gate implementations allow complex logic operations to be achieved in slightly over one basic logic gate propagation delay (τ_d) rather than two or three delays as would be the case for single level NOR or NAND implementations. They also dissipate less power and require less wafer area than single level circuit implementations.

In fact, such multi-level logic gate configurations may indeed be realized in SDFL with up to 3-level gates with many (10 - 20) inputs.[31] Logic gate designs of this type have been evaluated under a Rockwell IR&D program and details are presented in Ref. 31.

6.2 Circuit and Device Modeling

The size and complexity of the GaAs digital integrated circuits designed in this program has increased to the point where computer simulation and analysis are essential. It is important to have accurate and efficient models for circuit elements to predict circuit performances and to provide guidelines for circuit design and improvements in design rules. Almost any reasonable investment in computer time is preferable to designing and fabricating a nonfunctional or marginally functional circuit.

The success of the computer aided design depends critically on the model chosen for the active device. Normally, a complex model is capable of very accurate analysis. However, it may require excessive computation time and too much computer memory to accommodate the circuit. Ultimately, this will limit the size of the circuit and the application of the program.

The practical approach to computer aided design (CAD) is to utilize a number of levels of CAD analysis proceeding from detailed analysis of discrete active devices through highly modeled analysis of complex, many-gate (MSI or LSI) circuits. The key to this process is parameterization and modeling. For

example, the results of a detailed analysis of the GaAs FETs would be cast in the form of a model giving the values, and operating point variations of key parameters such as drain current, I_{gs} (V_{gs}, V_{ds}), gate capacitance, C_{gs} (V_{gs}, V_{ds}), feedback capacitance, C_{ds} (V_{gs}, V_{ds}), etc. This model can then be used (along with the models for diodes, active loads, etc.) with parasitic capacitance calculations to analyze logic gates of different configurations operating under different conditions of fanout, bias, etc. The results of this gate analysis is, then, a model for the gate itself with its own set of parameters and dependencies, such as rise time, fall time or propagation delay as a function of loading, bias, etc. Finally, these parameterized models for logic gates can be utilized in an overall analysis program for a complex MSI or LSI part. Clearly, considering the detailed electron dynamics in each GaAs FET of a 100-gate circuit (having several hudnred FETs or active loads) would be computationally prohibitive. By reducing the results of each level of analysis to a simple set of parameters, the variation of which are expressed with simple analytical formulas or "look-up tables," makes possible the use of the results in the next level of calculation, leading finally to the overall circuit analysis. Note also that the parameters at any level may be obtained from appropriate experimental measurements, if available, rather than calculations. For example, if propagation delay vs loading data are available for particular gate configurations, this can serve as the basis for MSI or LSI logic circuit analysis. The empirically derived results can also serve as a confirmation of the accuracy of the calculated model.

Thus, a three level CAD hierarchy was adopted for this program leading to the development of analytical and empirical device models for the MESFET and Schottky diode, a detailed circuit simulation program which uses the device model and is useful for MSI sized circuit blocks, and a logic analysis program useful for modeling LSI circuits and/or large functional blocks. In this section, each of these levels of CAD is described and examples of their application are presented.

6.2.1 Device Models

Two types of device models were developed and utilized. A simplified model, using first order analytical equations used experimentally-measured DC device parameters to define the appropriate constants and coefficients. Secondly, a more complex analytical model based on more detailed analytical descriptions of the MESFET device physics was developed by M. Shur and L. Eastman of Cornell University.

The diode model is shown schematically as an equivalent circuit in Fig. 6.2-1(a). The series resistance of the diode is represented by the linear resistor r_s. The dc characteristics of the diode are mainly determined by the nonlinear current source I_D. The value of I_D is determined by the equation

$$I_D = I_s \exp \frac{V_D}{nV_t} - 1 \quad . \tag{1}$$

where I_s is the saturation current, V_t is the thermal voltage equal to kT/q, and k is Boltzmann's constant. Also, T is the absolute temperature, in degrees Kelvin, and q is the electronic charge.

Capacitor Q_D models the charge storage in the junction depletion region of the diode.

$$Q_D = C_{jo} \int_0^{V_D} 1 - \frac{V}{\phi_B}^{-1/2} dV \quad , \tag{2}$$

where C_{jo} is the junction capacitance at zero bias voltage and ϕ_B is the built-in voltage. This charge-storage element can be equivalently defined by the capacitance relation

$$C_D = \frac{\partial Q_D}{\partial V_D} \tag{3}$$

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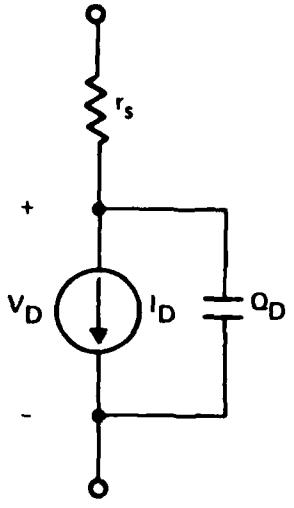
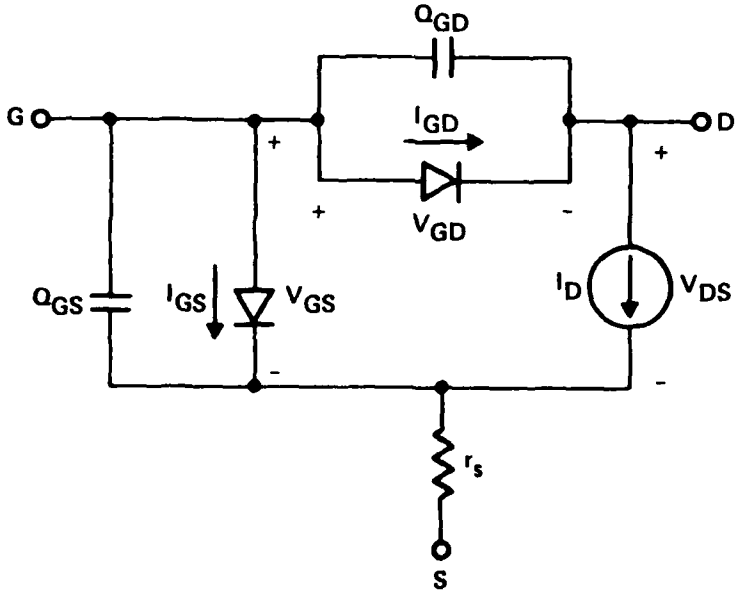


DIODE MODEL



FET MODEL

Fig. 6.2-1 (a) Diode model and (b) FET model.

The simplified MESFET model is shown schematically as an equivalent circuit in Fig. 6.2-1(b). The series resistance of the source region is represented by the linear resistor r_s. The dc characteristics of the FET are determined by the nonlinear current source I_D, whose value is given by the following equations:

$$I_D = 0 \qquad : V_{GS} - V_p \leq 0$$

$$I_D = K(V_{GS} - V_p)^2 - K(V_{GS} - V_p - V_{DS})^2 \qquad : 0 < V_{DS} < V_{GS} - V_p \text{ (linear region)} \qquad (4)$$

$$I_D = K(V_{GS} - V_p)^2 + g_D[V_{DS} - (V_{GS} - V_p)] \qquad : 0 < V_{GS} - V_p < V_{DS} \text{ (saturation region)} \qquad (5)$$

These equations provide good agreement to experimental data measured on low pinch-off voltage double-implanted MESFETs. Below saturation, a square law characteristic (or Shockley model) is used to fit the measured device I_{DS} characteristics as a function of V_{DS} and V_{GS}. Above saturation, the I_{DS} increase with V_{DS} is modeled by a linear drain conductance g_D. The agreement of these empirically derived dc equations with experimentally determined dc I_{DS} vs V_{DS} characteristics is shown in Fig. 6.2-2. Here, the calculated current values (points) are plotted on the same scale with measured data (solid lines). The charge storage in the gate junctions is modeled by the two nonlinear elements Q_{GS} and Q_{GD}.

$$Q_{GS} = C_{GSo} \int_0^{V_{GS}} 1 - \frac{V}{\phi_B}^{-1/2} dV \qquad (6)$$

$$Q_{GD} = C_{GDo} \int_0^{V_{GD}} 1 - \frac{V}{\phi_B}^{-1/2} dV \qquad (7)$$

C_{GSo} and C_{GDo} are the junction capacitances at V_{GS} and V_{GD} equal to zero, respectively. Alternatively, these two charges can be expressed as voltage-dependent capacitors C_{GS} and C_{GD}.

In the development of increasingly complex and more densely packaged circuits it is inevitable to have longer interconnect lines, more overcrossings and closely placed electrodes. Parasitic capacitances begin to play significant

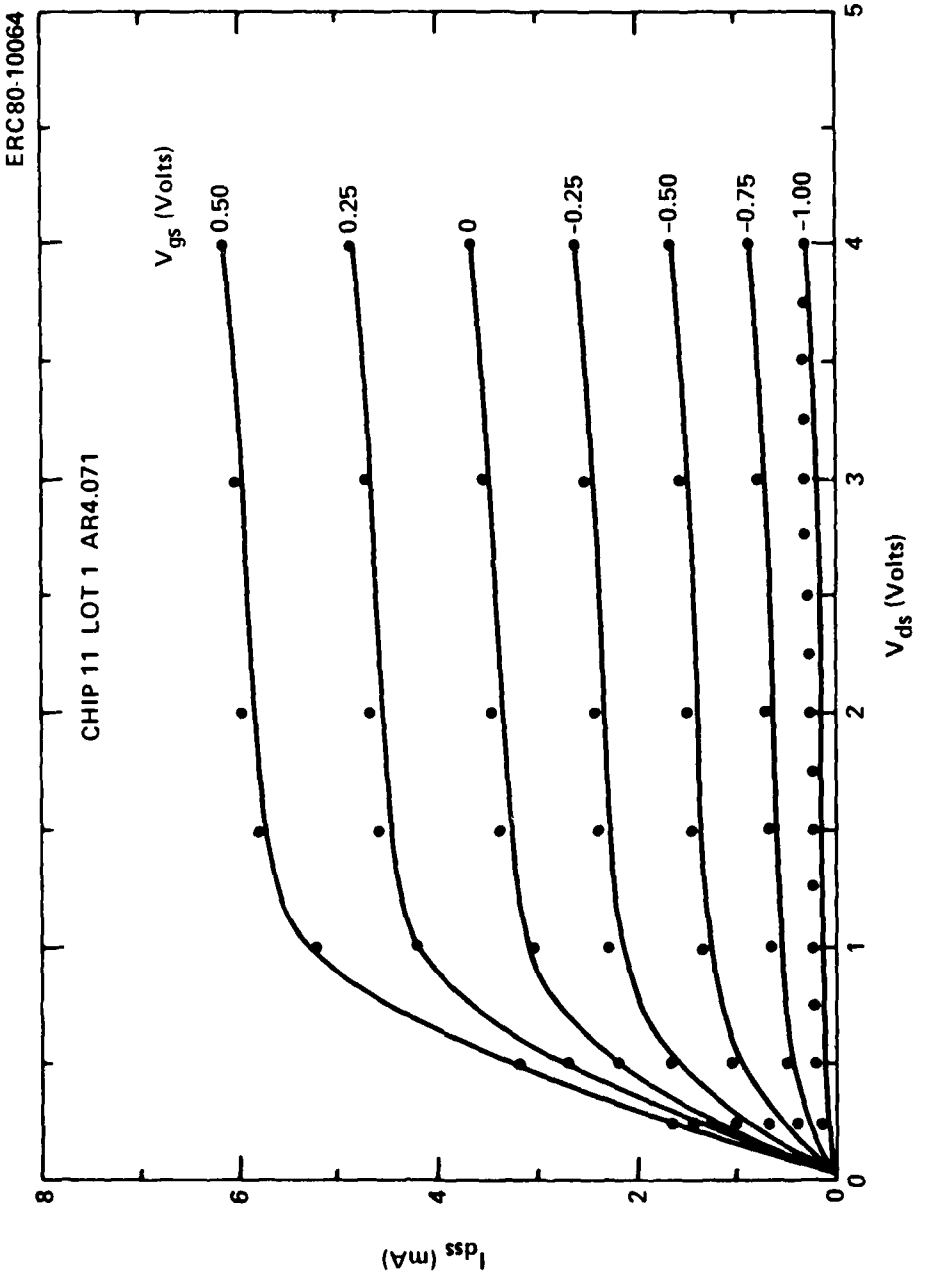


Fig. 6.2-2 Experimental (solid lines) and modeled (dots) I-V characteristic of a typical FET from an IC wafer.

roles in circuit performances. Therefore, good estimate of the microstrip capacitances, crossover capacitances, and geometrical capacitances, etc. becomes crucial in obtaining realistic simulation results. Figure 6.2-3 shows the SDFL gate sub-circuit with fringing capacitances C_1, C_2, C_3, C_4, C_5, C_6, and C_7. The microstrip capacitance C_p of the output of each gate can be calculated based on the geometry of the interconnect line. An estimate of C_p for a line width of $w = 1.5$ μm and a substrate thickness of $H = 635$ μm leads to 0.05 ff/μm.

6.2.2 Cornell Device Model

A more complex analytical parameterization of the MESFET device has been carried out at Cornell University. As a result of their efforts, two models of a GaAs MESFET (computer and analytical) have been developed. The main emphasis was to develop an analytical model which takes into account all important physical effects but requires small computation times.

Both computer and analytical models may be considered as a compromise between the simple qualitative description of FETs (as described in 6.2.1) which is provided by the Shockley theory, and a rigorous computer analysis. The Shockley theory gives physical insight into FET operation and provides a reasonable agreement with experimental data for low pinchoff voltage devices with gate lengths 1 μm or greater but is not accurate for shorter channel devices nor does it provide quantitative information on small signal ac parameters because the hot electron effects are not adequately included. A rigorous two-dimensional analysis, on the other hand, requires very large computer time and is hardly suitable as an on-line computer-aided design tool.

The computer model developed at Cornell requires very small computation time (0.25 seconds per point of current voltage characteristic) but it is based on the physical picture revealed by a rigorous two-dimensional computer analysis.

The main features of the model are:

1) It divides the MESFET into three sections (a) source-gate portion which is assumed to behave like an ohmic resistance (b) a channel

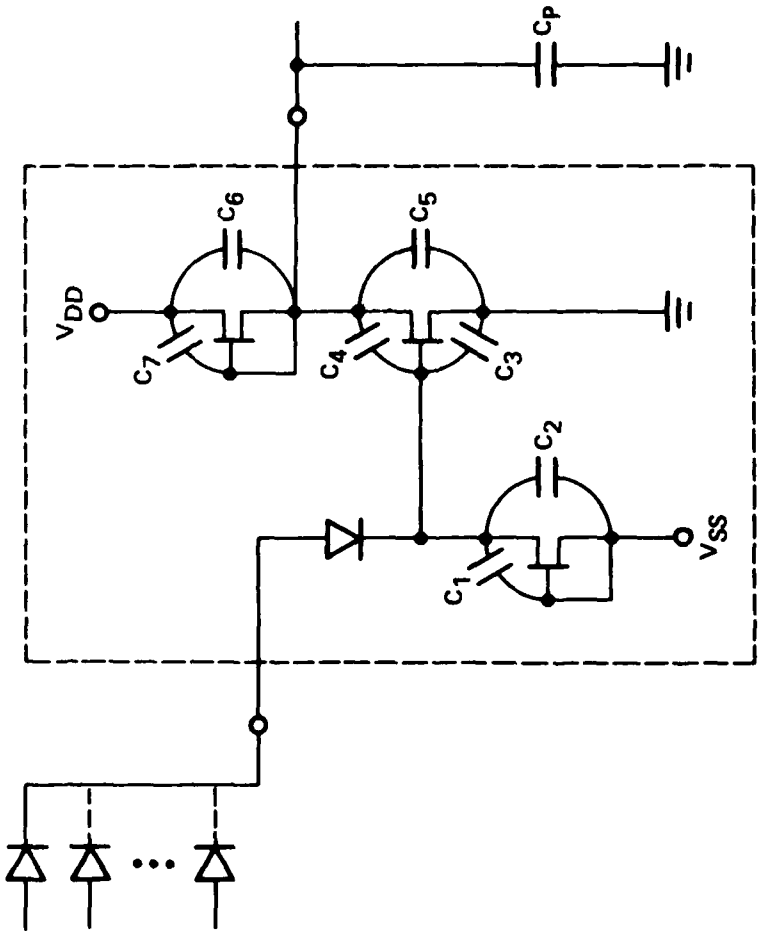


Fig. 6.2-3 SDFL NOR gate sub-circuit.

under the gate, (c) an adjacent Gunn domain, extending toward the drain, which can form if the electric field at the drain side of the channel is larger than a domain sustaining field.

2) The x-component of the electric field under the gate is always smaller than the electron velocity-peak field E_p. The heating of electrons under the gate is thus negligibly small.

3) The carrier concentration changes gradually at the boundary of the depletion layer due to diffusion effects. This distribution is approximated by a sinusoidal function, and a two-dimensional solution of Poisson's equation for the approximated carrier distribution is used.

4) The drain current, I_{DS}, is composed of two components, the channel current I_{ch} flowign through the channel and the Gunn domain, and a leakage current I_s in the non-ideal interface and substrate regions which have an effective shunt resistance.

5) The ohmic resistances of the gate-source and gate-drain portions and contact resistances are considered in series with the channel and the Gunn domain.

This model was applied to a calculation of current-voltage characteristics, switching time and small-signal parameters of GaAs FET (such as transconductance g_m, and gate-to-source capacitance C_{gs}) finding good agreement with the results of a two-dimensional computer analysis.[32] A much more detailed description of this work has been reported by Shur and Eastman.[33]

Although the above model can be used for CAD, efforts were made toward further simplification by developing an analytical model, with simple analytical expressions for switching times and power delay products. This first analytical model assumed uniform channel doping. Device dc and ac small signal device parameters could also be obtained through the evaluation of simple analytical

expressions. Details describing this model and its predictions have been reported by Shur.[34] Good agreement between device parameters (I_S, g_m, C_{GS}, and C_{GD}) calculated by this model and measured on relatively high pinchoff voltage microwave MESFETS has been demonstrated.[35]

Efforts have been made to compare the predictions of the analytical model with available measured FET parameters on the low pinchoff, double-implanted devices used in the SDFL logic gates. An example of one such comparison derived from I_{DS} vs V_{GS} data from FETs on a wafer is shown in Fig. 6.2-4. In this figure, the solid line represents the predicted transconductance derived from the Cornell model[36]

$$1/g_m = (1 - r/2)\ 2V_p/I_{FC} - 2V_pI_{DS}/I_{FC}^2 \tag{8}$$

where V_p is the pinchoff voltage, I_{FC} is the calculated full channel current and $r = R_{source}\ I_{FC}/V_p$. The circles represent data points taken from the wafer. Good agreementr with the analytical model is shown in the high I_{DS} saturation region. However, in the region near pinchoff (broken line) departure from the theory is evident. In this region (near threshold), where $V_{gs} - V_p < 1$ V, a simple square law model

$$I_{ds} = K(V_{gs} - V_p)^2 \tag{9}$$

provides a better fit to the experimental data.

Therefore, the analytical model was modified to provide better quantitative agreement with the dc experimentally determined characteristics of low pinchoff voltage MESFETs designed for logic circuit use. To accomplish this, a nonuniform doping profile typical of ion-implanted FET channels was incorporated into the model. Equations limiting the transconductance (g_m) vs V_{GS} and I_{DS} vs V_{GS} characteristics with the doping profile were solved. Improved agreement in the $V_{GS} - V_p$ = 0.5 to 1.0 V range was observed.

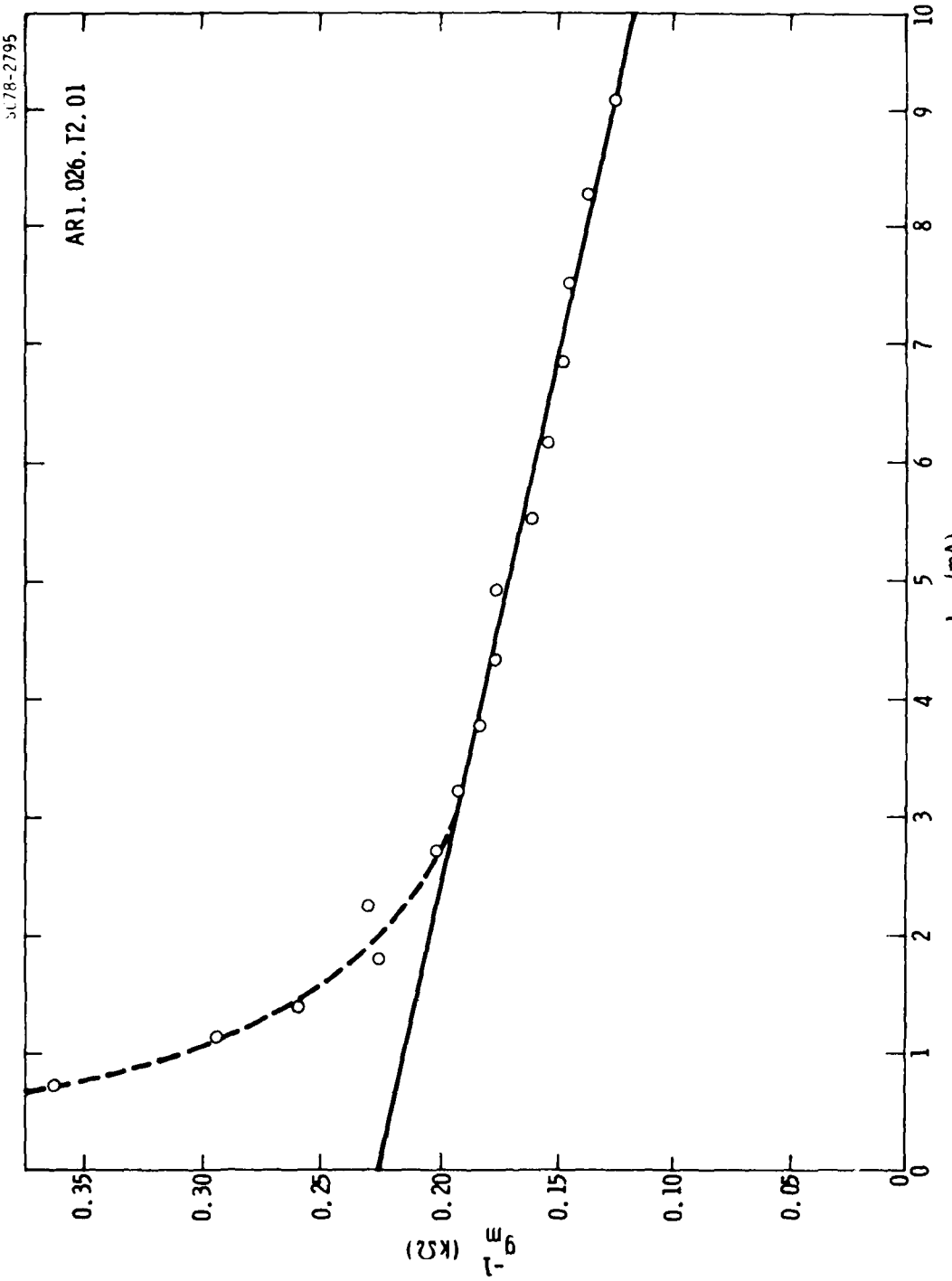


Fig. 6.2-4 Plot of g_m^{-1} vs I_{DS} comparing analytical model (solid line) with low power FET measured data points.

Further modifications were then implemented on the nonuniformly doped FET model to include the effect of source resistance on the predicted I_{ds} vs V_{gs} and g_m vs V_{gs} characteristics. In addition, the model was adapted so that a modified Shockley (gradual channel approximation) model is utilized when the device reaches current saturation due to pinch-off rather than velocity saturation. In this non-velocity saturated region,

$$V_T + V_{gs} - I_{ds} R_s < V_s \tag{10}$$

where V_T is the pinch-off voltage referred to the device terminals, R_s is the source resistance, and V_s is the voltage drop across the portion of the channel under the gate at saturation. Above the limit of carrier velocity saturation, the previously reported analytical model, modified for nonuniform doping, was utilized. Finally, for the case of low pinch-off devices typically used in digital logic applications, an ion implanted doping profile model was derived. This profile approximately reconstructs the doping distribution close to the surface by fitting $N_d - N_a$ from C-V data measured on the doping tail.

The above modificationsd have resulted in much improved agreement with experimental FET data, particularly for higher pinch-off devices. Figure 6.2-5 shows the calculated and experimental g_m vs V_{gs} for a 50 μm wide FET with relatively high (-1.5 V) pinch-off voltage. This was calculated by the non-hybridized saturation model without including source resistance.

Figure 6.2-6 also presents the transconductance g_m, this time for the modified model. Curve 4 represents experimental data while curve 1 represents the nonuniform profile without R_s, and curve 3 the uniform profile without R_s. Also, Fig. 6.2-7 presents I_{ds} vs V_{gs} for the same profile and model variations. As can be seen from the two figures, the nonuniform hybridized model with source resistance (curve 1) provides the best agreementr with the experimental results. All factors seem to be essential in providing this agreement (R_s, nonuniform doping, and the transition to the Shockley model at low V_{gs}).

The calculations was also carried out for a device with low pinch-off voltage (-0.6 V). The estimated profile was reconstructed from doping informa

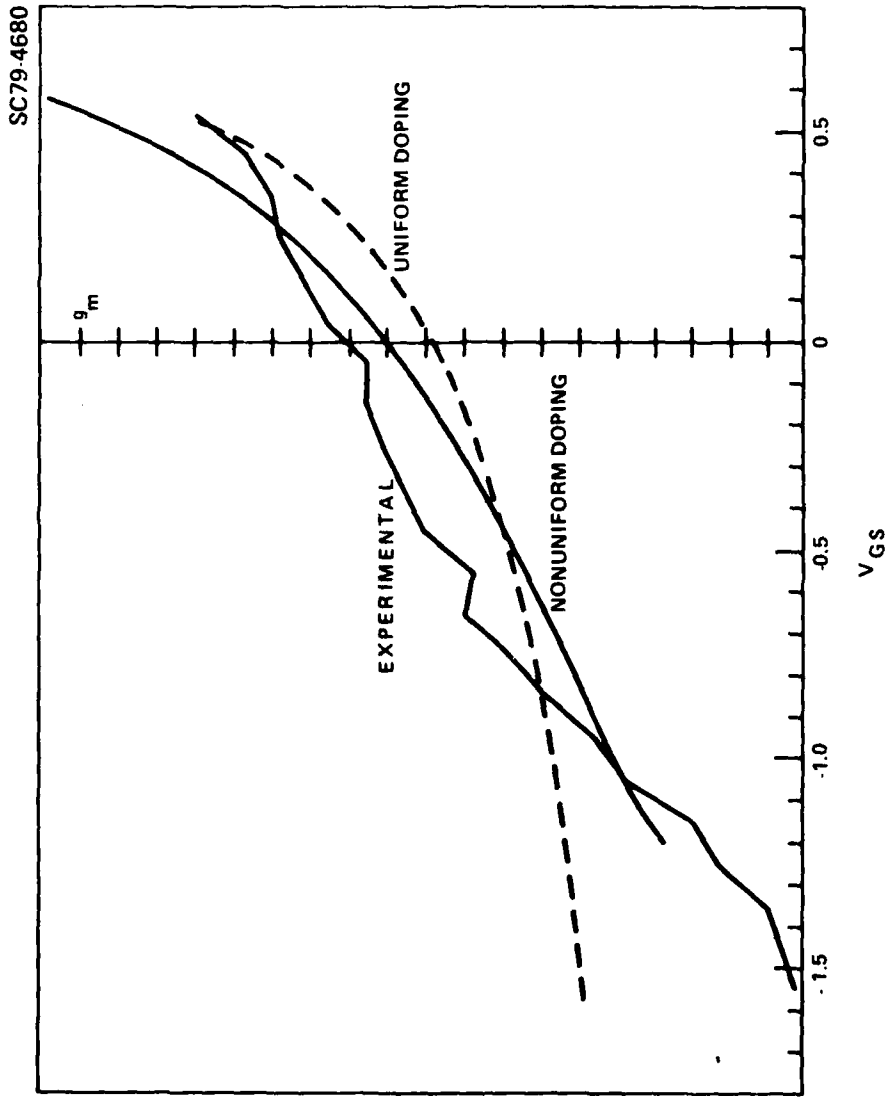


Fig. 6.2-5 Transconductance as a function of gate-source voltage for a 50 μm FET. Calculated transconductances are shown for both the uniform and non-uniform doping profiles (from Ref. 1).

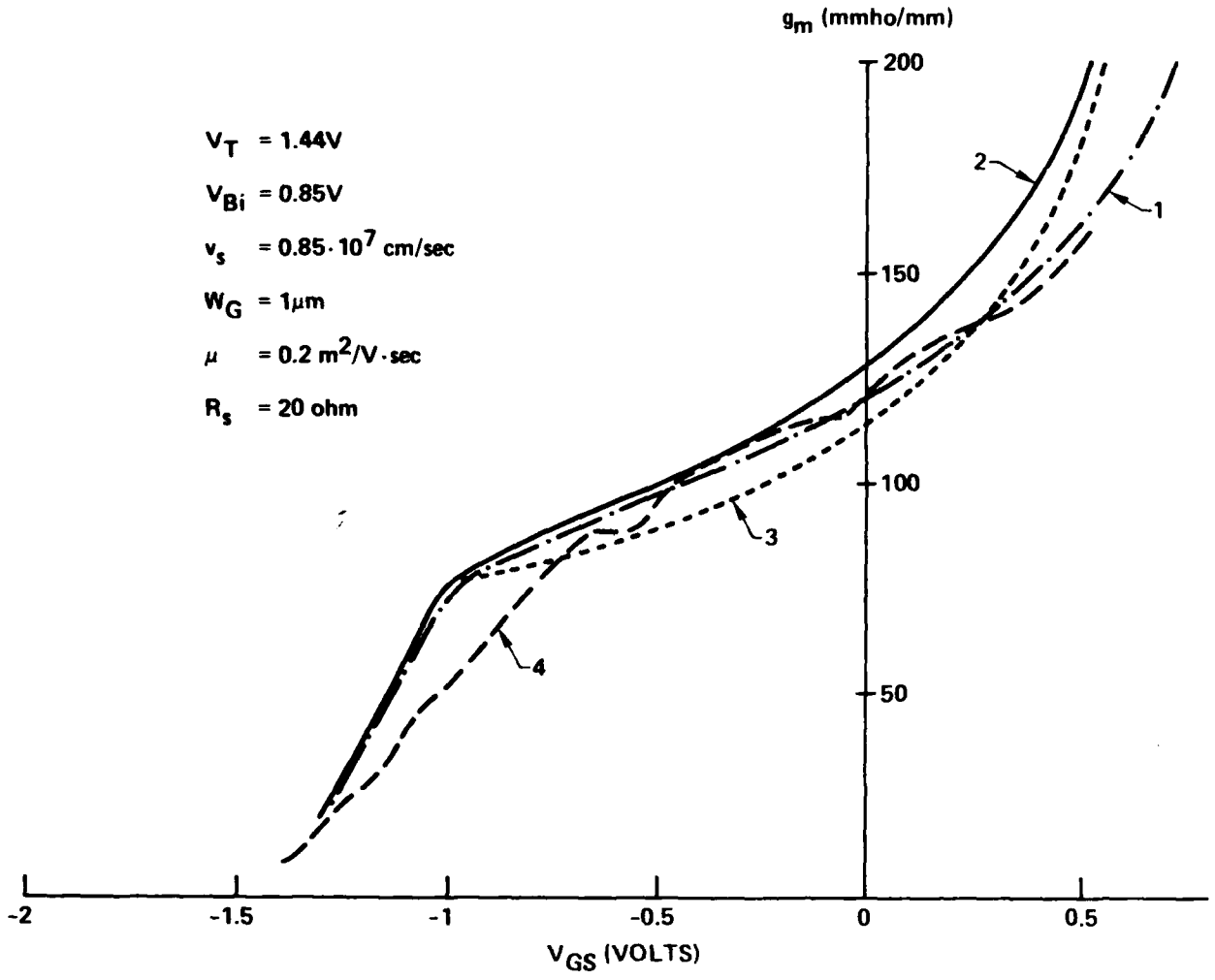


Fig. 6.2-6 Transconductance vs gate-source voltage for a 50 μm FET. 1. Non-uniform profile, R_s included; 2. Non-uniform profile, R_s not included; 3. Flat profile, R_s not included; 4. Experimental data.

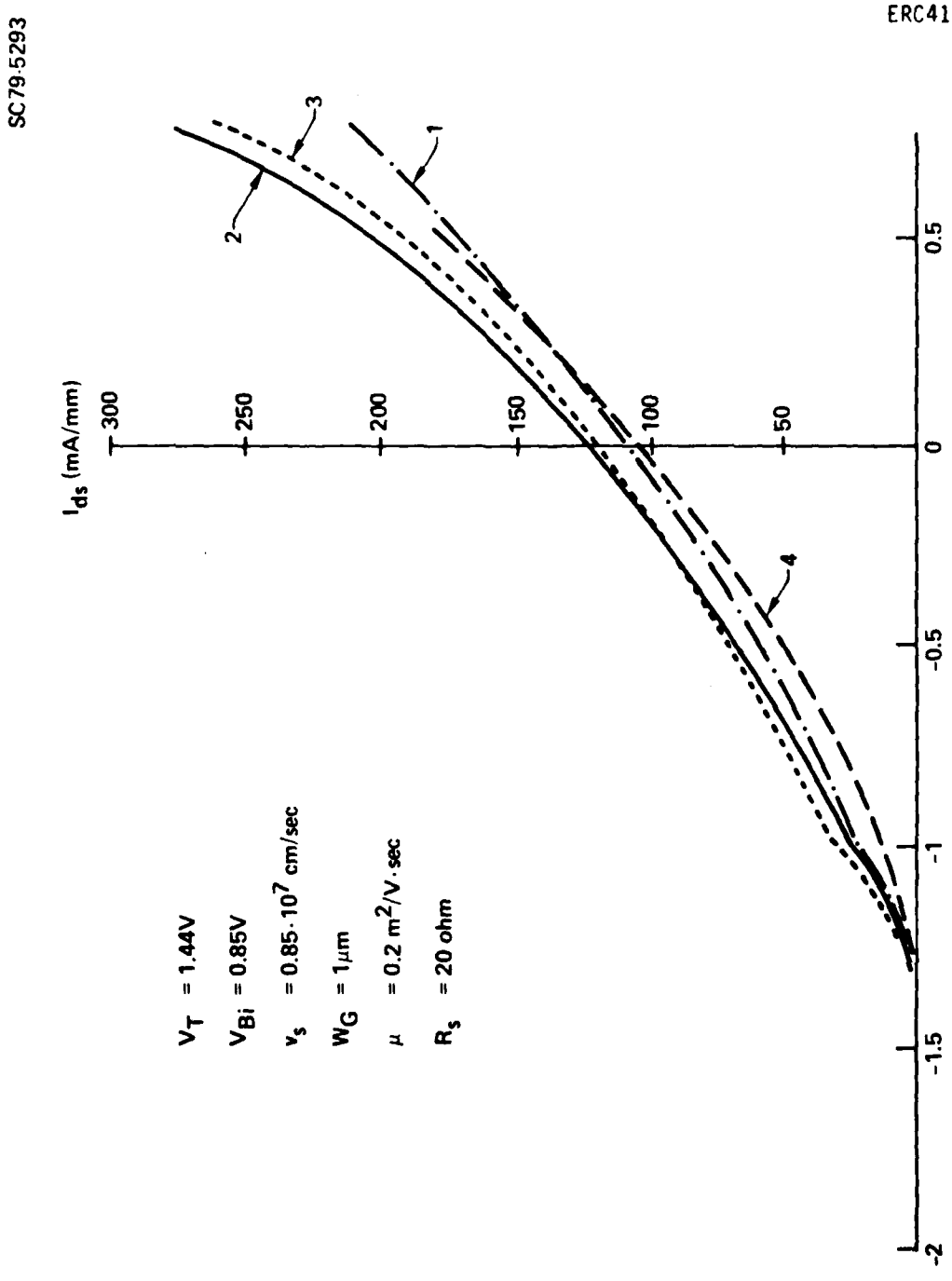


Fig. 6.2-7 Saturation current vs gate-source voltage for a 50 μm FET. 1. Non-uniform profile, R_s included; 2. Non-uniform profile, R_s not included; 3. Flat profile, R_s not included; 4. Experimental data.

tion measured on the tail of the implant. Figures. 6.2-8 and 6.2-9 compare calculated and experimental data on the transconductance and drain-source current as a function of V_{gs}. The same model variations discussed above were used on these plots as were discussed above. Here, the agreement is not quite as good, with a tendency for the calculated I_{ds} to exceed the experimental I_{ds}. This may indicate a smaller effective saturation velocity compared to the higher pinch-off case, or a greater dependence of the effective velocity on the voltage across the channel.

Additional details describing the non-uniformity doped model have been reported by M. Shur and L. Eastman.[37]

6.2.3 Circuit Simulation Program

The general purpose circuit simulation program SPICE II (version 2E.2), which was developed by the Integrated Circuits Laboratory at the University of California, Berkeley, was selected for use in the GaAs digital IC modeling effort. The program was modified for use on the CYBER 176 computer available at Rockwell. In addition, since the diode and JFET models in SPICE II were designed for typical silicon devices, modification of these models was necesasry to accurately represent GaAs device parameters. The models described in Section 6.2.1 were implemented as subroutines for use in this program. Sample runs were prepared and their simulation results were compared with the experimentally measured diode and FET characteristics to determine the appropriate value of various model parameters. The sub-circuit consisting of one SDFL gate shown in Fig. 6.2-3 was then established by combining device models of switching diode, level shifting diode and FETs. This SDFL gate sub-circuit is the basic unit for subsequent simulations of more complex circuits.

In the SPICE II program, each element in the circuit is represented by a mathematical model, and a system of algebraic-differential equations describing the complete circuit is determined by the model equations for each element and the topological interconnections of the elements. The iterative equation solving algorithm may require excessive cpu time and sizeable computer memory

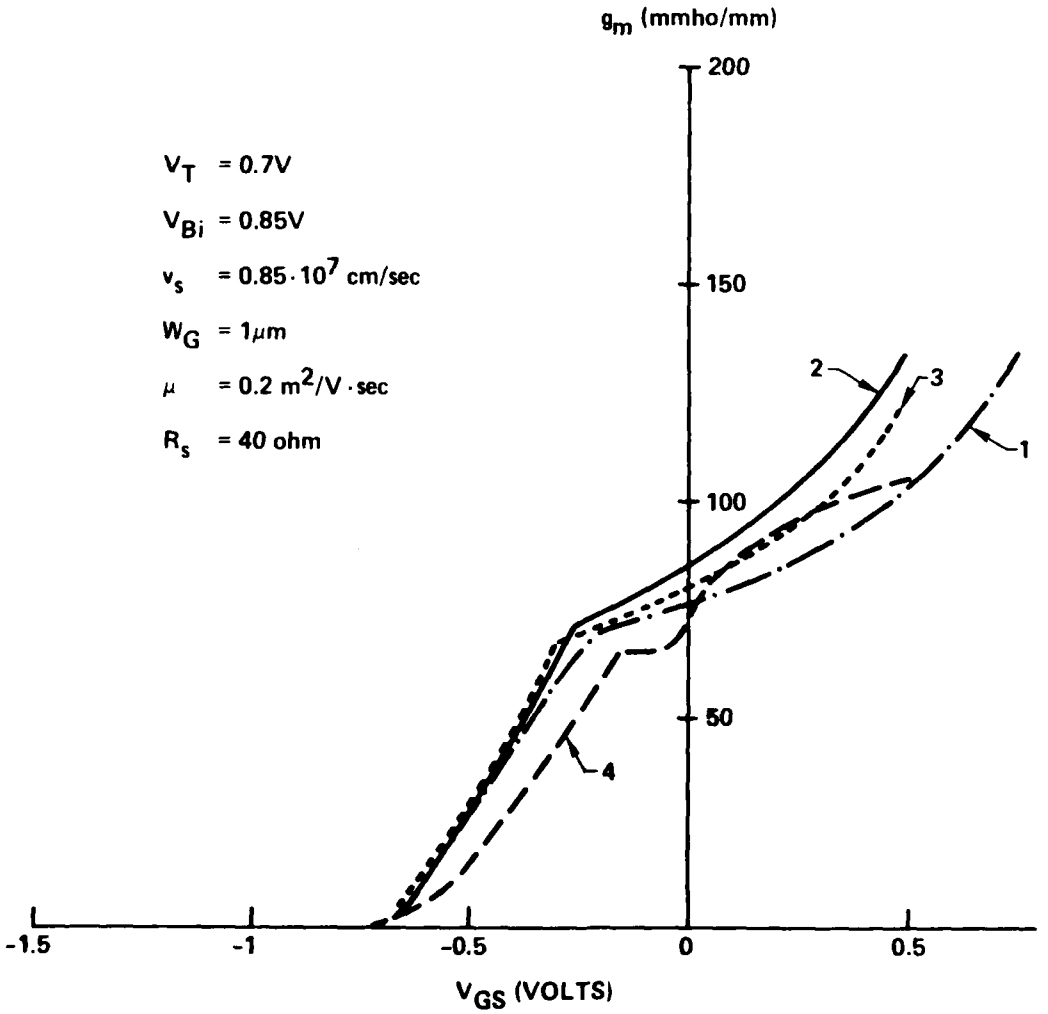


Fig. 6.2-8 Transconductance vs gate-source voltage for a low-pinchoff voltage 50 μm FET. 1. Non-uniform profile, R_s included; 2. Non-uniform profile, R_s not included; 3. Flat profile, R_s not included; 4. Experimental data.

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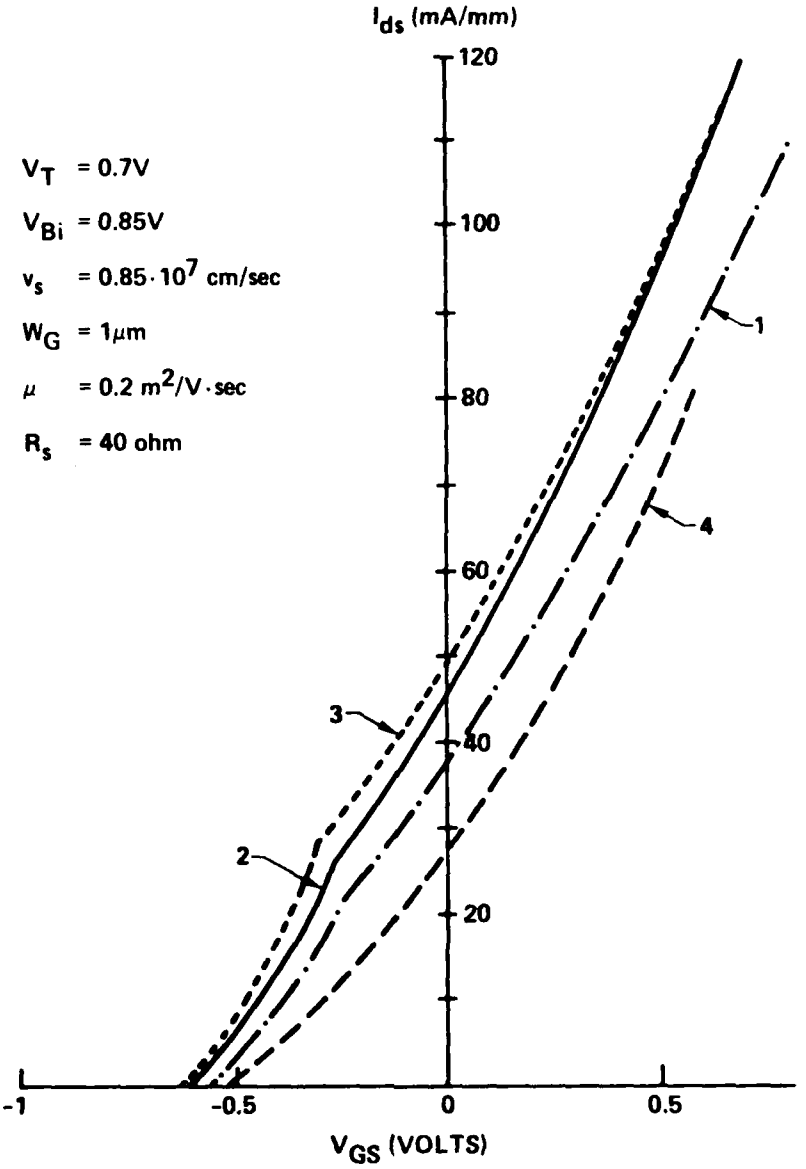

Fig. 6.2-9 Saturation current vs gate-source voltage for a low pinchoff voltage 50 μm FET. 1. Non-uniform profile, R_s included; 2. Non-uniform profile, R_s not included; 3. Flat profile, R_s not included; 4. Experimental data.

for simulation of very large circuits. For reasonable computer expenses it appears desirable to use SPICE II to simulate circuits with up to 50 gates.

For circuits with more than 50 gates, SPICE II becomes computationally prohibitive, while the detailed analysis it provides is not required because large circuits are usually made up of functional "blocks," which have already been modeled in detail. Therefore, large circuits are modeled at a higher level of analysis hierarchy using the logic simulation program described in Section 6.2.4.

Figure 6.2-10(b) shows the simulated output waveform of a 10 μm SDFL NOR gate responding to the input waveform shown in Fig. 6.2-10(a). Figure 6.2-11 shows the simulation result for a 3 stage ring oscillator with 10 μm SDFL NOR gates. By varying the supply voltages V_{dd} and V_{ss}, the gate propagation delay obtained from simulations ranges from 82 ps to 124 ps. This is in reasonable agreement with typical experimental results. On wafers from mask set AR1 and AR2, the best propagation delay evaluated from ring oscillators with 10 μm SDFL NOR gates and with moderate pinch-off voltage (1.2 V) was 95 ps. On AR3, as low as 62 ps was observed (see Table 6.1-1).

A D flip-flop was simulated at 1.6 GHz clock frequency. The output waveforms are shown in Fig. 6.2-12. This is again in good agreement with the experimental data from the 3 stage D flip-flop divider of mask set AR3 which exhibited a maximum clock frequency of 1.9 GHz (see Section 6.3).

The circuit simulation results discussed in this section agree with reasonable accuracy with measured data. Enough confidence has been gained to use our current analytical models in detailed investigation of more complex circuits and to evaluate circuit design alternatives. However, further improvements in device models are needed to refine this capability, particularly in the area of bias dependences of FET capacitances, since the assumptions made here have a strong impact on the logic gate speed predictions.

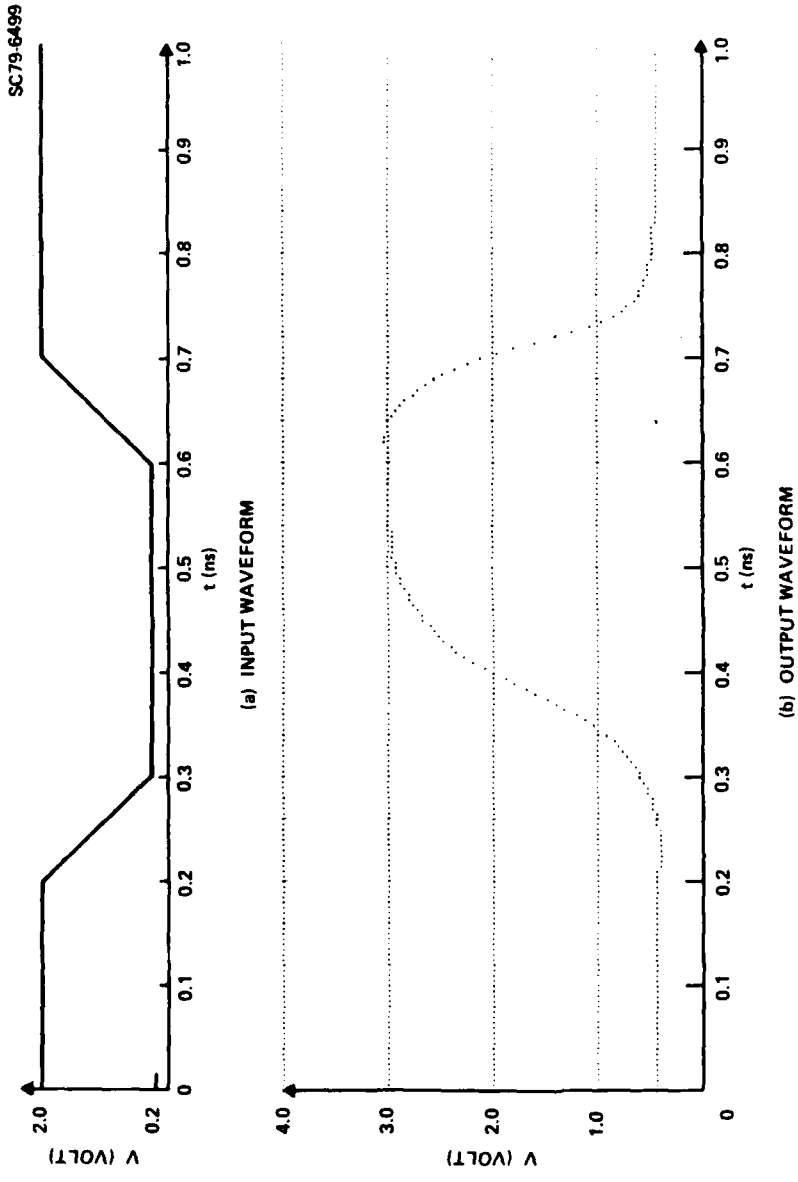

Fig. 6.2-10 Simulated transient response of an SDFL NOR gate.

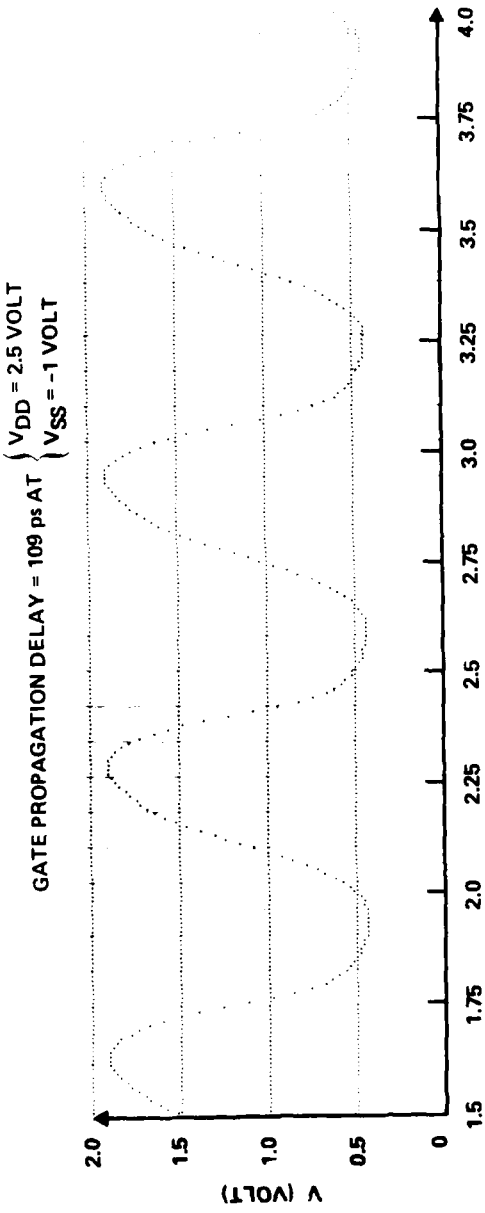

Fig. 6.2-11 Simulation output for a 3-stage ring oscillator.

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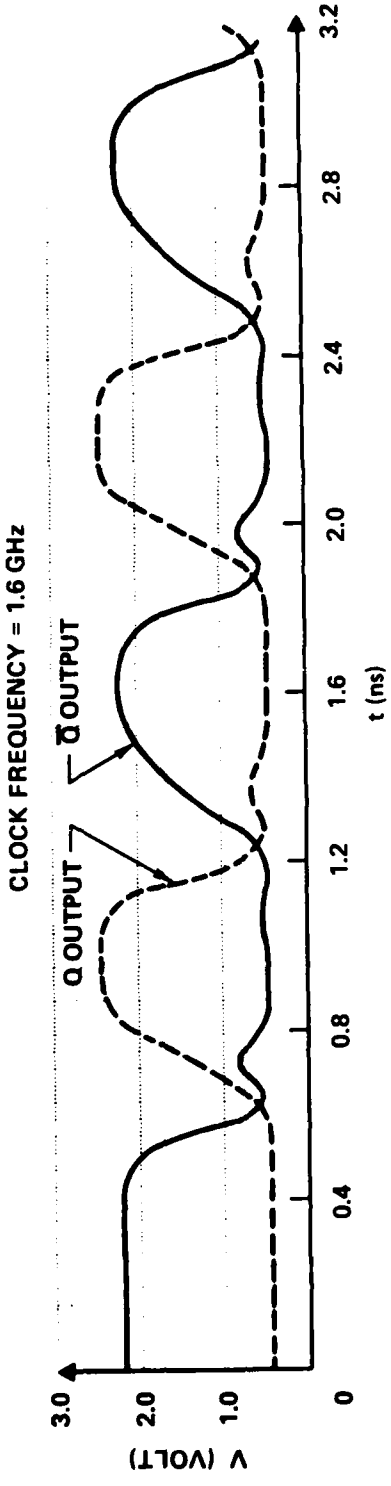

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Fig. 6.2-12 Simulation output for a D flip-flop.

6.2.4 Logic Simulation Program

To cope with the very practical circuit design problems involved in designing new mask sets for this program, a complex (MSI-LSI) logic circuit analysis program, representative of the "highest level" of this CAD analysis hierarchy has been developed. This program, written in 6502 assembly languagre for an APPLE II microcomputer, utilizes a look-up table parameterization for the GaAs SDFL NOR or OR/NAND logic gates. In the present form, the program uses a single look-up table defining the output voltage slew rate for an SDFL gate as a function of its input voltage. This assumes that all gates are scaled for equal risetimes and propagation delays with their various loadings. Minor program changes could eliminate this restriction. The calculation is a full iterative analog calculation of the response of up to 128 SDFL NOR gates or 64 OR/NAND gates of up to 5 inputs each (expandable). The iteration interval is taken as 1/20 of a propagation delay (or about 3.8% of the slew time) for good accuracy and assured convergence. Because it is a full analog calculation, the results cleraly show incipient "glitches" as maximum clocking rates are approached.

The program has been used to analyze the circuits designed as demonstration vehicles (see Sections 6.3 and 6.4). As an example, some simulated results for a 3 stage synchronous counter with decreasing driving clock frequencies are given. The circuit diagram of this counter is shown in Fig. 6.2-13. It consists of three D flip flops and some NOR gates, for a total of 23 NOR gates. The clock input and the outputs from the three stages are shown in Figs. 6.2-14 and 6.2-15 for four clock rates. At the highest clock rates (Figs. 6.2-14(a) and 6.2-14(b)) the responses are not correct, except for the output from the first stage which appears as the clock signal divided by two. At slightly lower clock rates (Figs. 6.2-15(a) and 6.2-15(b)) the simulation generates proper outputs, each one appearing as the output from the previous stage with the frequency divided by two. Observing the small glitch in the waveforms of Q_2 and Q_3, one can state that the case in Fig. 6.2-15(a) is near the threshold for proper operation. Therefore, the maximum clock frequency is 1/5.1 τ_D, τ_D being the propagation delay per gate. The above circuit analysis was performed in 8 seconds of computer time. The simulated output waveform of each gate in the

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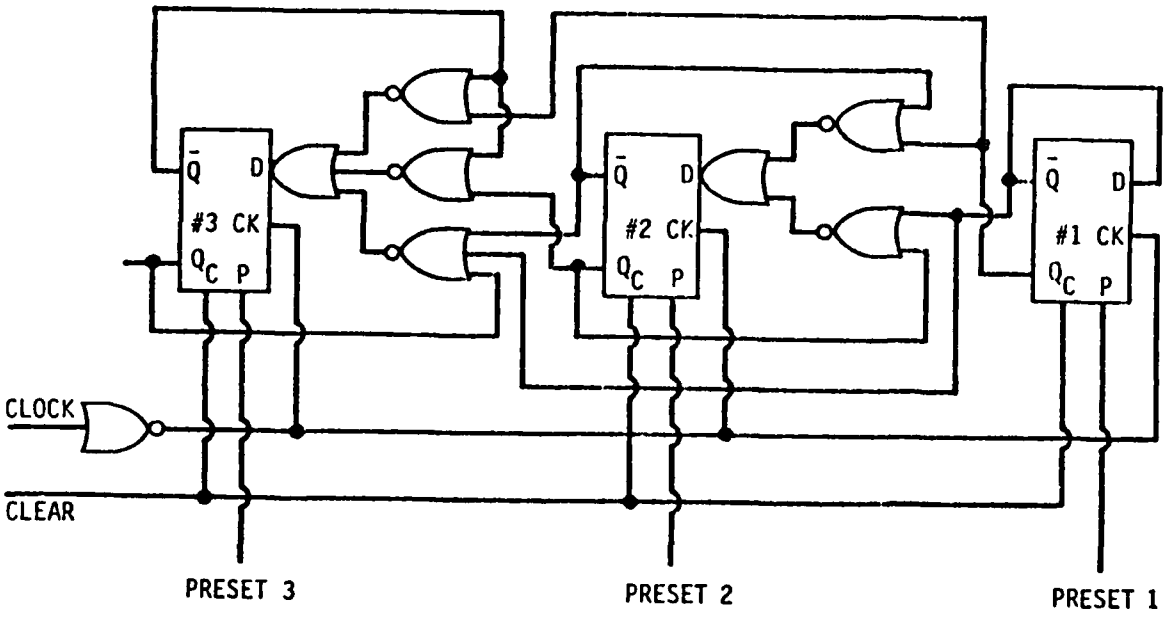

Fig. 6.2-13 Circuit diagram for a 3 stage synchronous counter.

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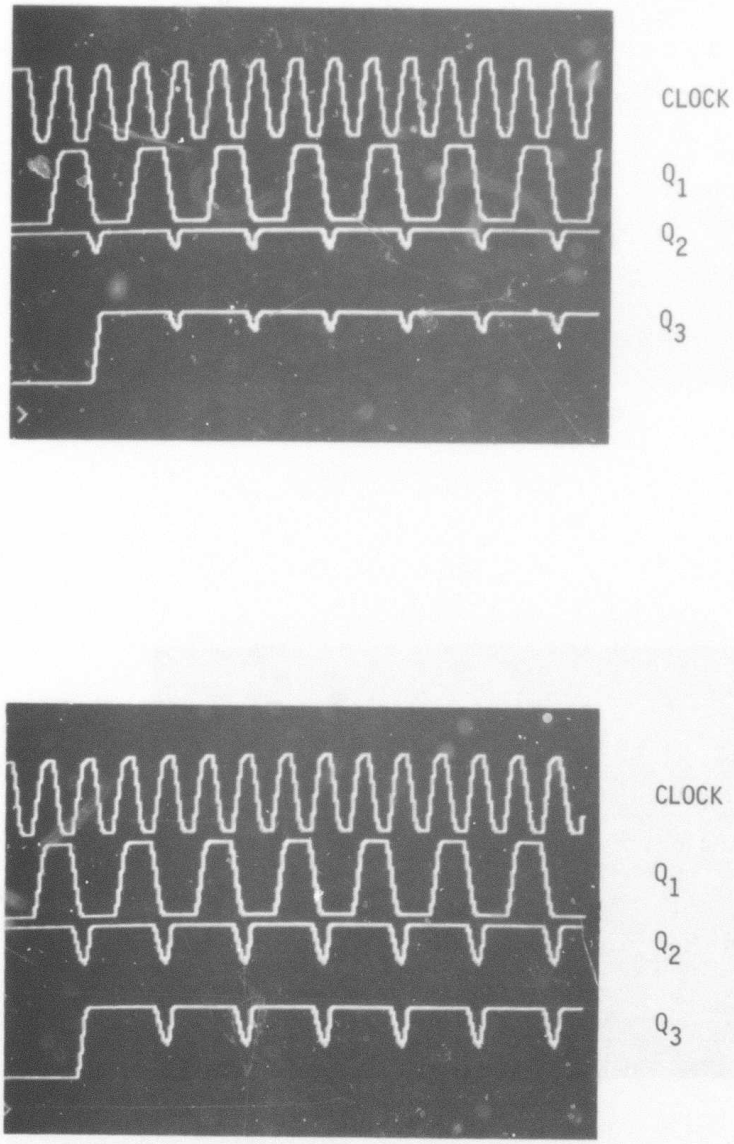
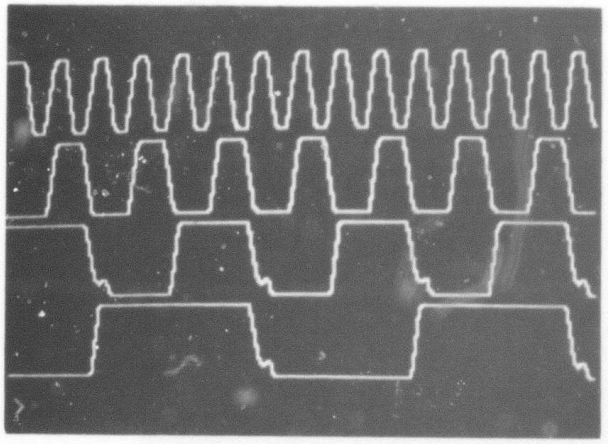


Fig. 6.2-14 (a) 3 stage synchronous counter with clock frequency at $1/5\tau_D$ (b) 3 stage synchronous counter with clock frequency at $1/5.1\tau_D$.

SC78-1238



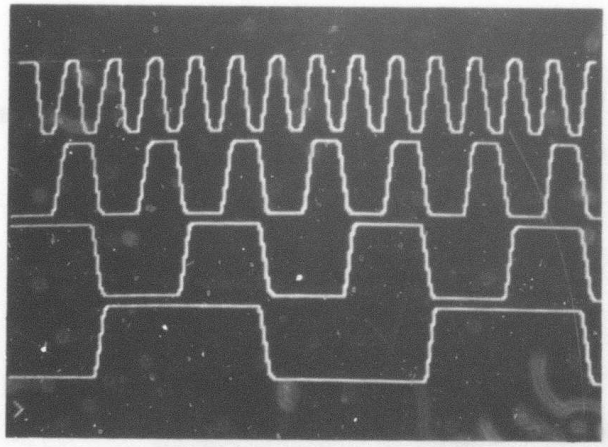


Fig. 6.2-15 (a) 3 stage synchronous counter with clock frequency at $1/5.2\tau_D$ (b) 3 stage synchronous counter with clock frequency at $1/5.3\tau_D$.

circuit can be easily obtained from this logic circuit analysis program. This information is very important for the verification of the proper operation of each gate in the actual devices when tested.

6.3 MSI Circuit Performance Summary

While ring oscillators are useful devices for measurement of the basic speed-power properties of logic gates, a more realistic index of performance is provided by the operation of gates in real sequential or combinatorial logic circuits. In these circuits, high speed performance is generally determined by worst case gate delay, using gates with average fan-ins and fan-outs of 2 to 3. For this study, the D flip-flop was chosen as a representative example of sequential logic circuits because of its general usefulness in frequency dividers, counters, shift registers and data latches. Parallel multipliers, implemented with half and full adders, were selected as an MSI and LSI combinatorial logic circuit examples, and are discussed in Section 6.4. All high speed measurements described in these sections have been made at wafer probe level. Output buffers (source followers) are located on-chip to prevent loading of the circuit during testing. Preliminary work on circuit packaging is discussed in Section 6.5.

Frequency Dividers

Binary ripple counters or frequency dividers have been made using the D Flip-Flop (DFF) as a basic building block. The DFF contains 6 NOR gates interconnected to form 3 set-reset latches as shown in Fig. 6.3-1. By connecting the D (data) input to the $\overline{Q}$ output, the clock input will produce an output transition for every full clock cycle. Thus, each DFF stage divides by 2. The propagation delay per gate can be inferred from the maximum experimentally observed toggle frequency when compared with the results of a logic analysis modeling program. The program indicates that correct operation should be maintained up to $f_c = 1/(4.85\ \tau_D)$, where τ_D is the maximum propagation delay for a logic gate in the circuit.[37]

Three stage dividers (÷8) containing 25 NOR gates have been fabricated using three such D Flip-Flops. A buffered output is taken from each stage to

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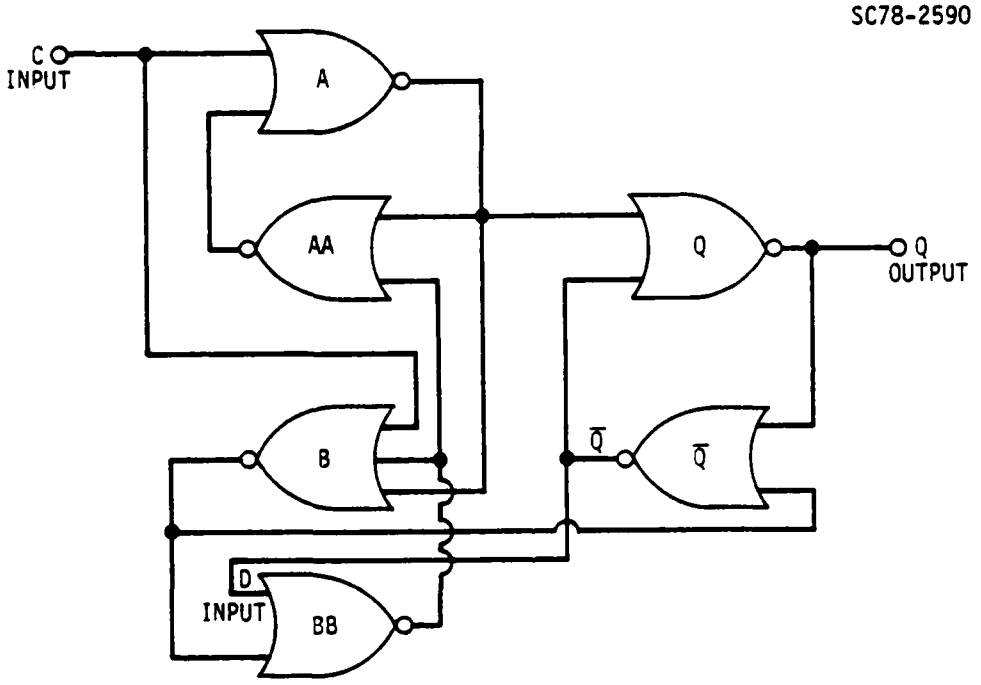

Fig. 6.3-1 Schematic diagram of a T-connected D-flip flop.

provide ÷2 and ÷4 outputs as well as a ÷8 output. This is illustrated in Fig. 6.3-2 where the divided outputs are shown with 100 MHz clock input used for this test. The three stage divider circuits have also operated up to a clock frequency of 1.9 GHz. Figure 6.3-3 shows the ÷8 output at 237 MHz from the divider operating at 1.86 GHz. This corresponds to an equivalent propagation delay of 110 ps, in good agreement with ring oscillator data for 10 μm SDFL NOR gates. The observed dynamic switching energy varied between the 0.25 to 0.45 pJ/gate, depending on the bias conditions and wafer pinch-off voltage. Power dissipation ranged from 45 to 145 mW for the three stage dividers.

In interpreting the significance of these results, it is especially important to recognize that the D Flip-Flop was chosen for the ripple divider because of its general usefulness as a building block for more sophisticated logic circuits, not because it provides a particularly high speed frequency divider. Other circuit approaches, such as complementary-clocked master slave divider are architecturally superior as microwave frequency dividers, since the same 110 ps propagation delay would, in that circuit, yield a maximum clock frequency of nearly 4 GHz, albeit at the expense of more difficult clocking requirements.[29] The main accomplishment of the DFF ÷8 measurements is the demonstration of very low effective gate propagation delays under fan-out and fan-in of 3 loading conditions, in a circuit with critical timing paths.

These devices have also been packaged in 16 pin flat-packs and delivered under the present program as demonstration circuits. Performance in the 1 to 1.8 GHz maximum clock frequency range was observed on the packaged divider circuits. Circuit packaging will be discussed in more detail in Section 6.5.

While statistical yield data has not been gathered on high speed circuits on a regular basis, an acceptable data base is provided by the results of probing frequency dividers in order to map wafers for potential deliverables. These dividers are no longer on the forefront of the development programs in terms of complexity but they are proven MSI circuits with reasonable gate counts. Divide by ÷8 circuits were mapped. These were contained on wafers fabricated on mask AR3 having 32 chips/wafer. The yields are summarized in Table 6.3-1.

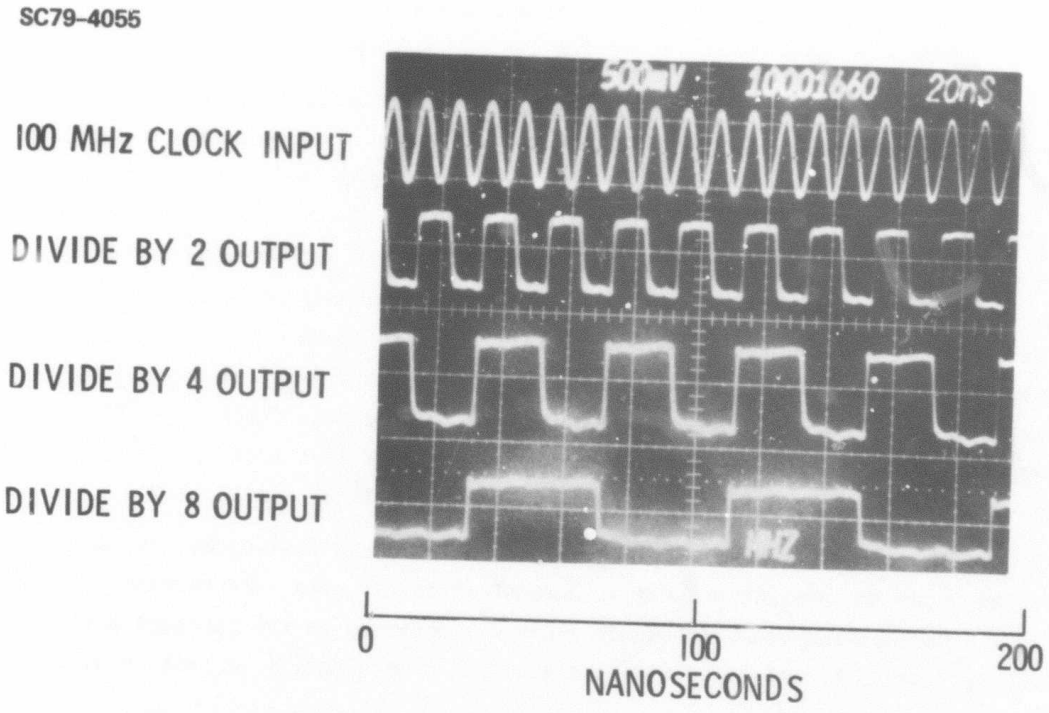

Fig. 6.3-2 3 stage D flip-flop divider operation at 100 MHz clock frequency.

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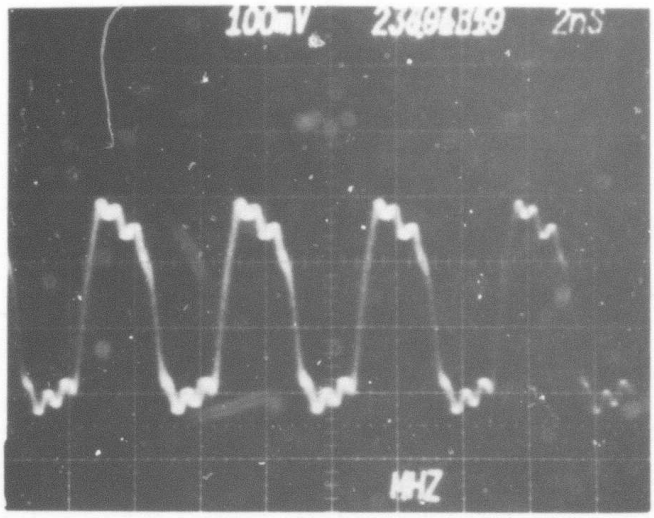

DIVIDE BY 8
OUTPUT

0 10 20
NANOSECONDS

3 STAGE D FLIP-FLOP DIVIDER OPERATION AT 1.9 GHz CLOCK

POWER DISSIPATION = 145 mW

DYNAMIC SWITCHING ENERGY = 0.48 pJ/GATE

PROPAGATION DELAY = 110 ps/GATE

Fig. 6.3-3 3 stage D flip-flop divider operation at 1.9 GHz clock.

Table 6.3-1
Yield of Frequency Dividers (:8)

Wafer	No. Working	Yield
AR3-69	14/32	44%
AR3-71	14/32	44
AR3-79	11/32	34
AR3-81	24/32	75

These are quite satisfactory yields. However, these were tested on the AR3 wafers judged to be the most promising available, the main selection criteria being pinchoff voltage values and uniformity of the dc device parameters.

Finally, Table 6.3-2 presents a statistical analysis of the uniformity of divider performance observed in testing the four AR3 wafers at probe. The average and standard deviations of the maximum clock frequencies are indicated here with some correlation evident between pinchoff voltage and maximum clock frequency. Wafer AR3-69 was probably limited in speed by the probe card itself which experienced severe resonance effects around 1.4 GHz.

Multiplexer/Demultiplexer Circuits

Large MSI circuits including an 8-input data multiplexer containing 64 gates have been evaluated.[38] This circuit would be useful, for example, for parallel-to-serial conversion or a high speed gigabit data transmission link. A logic diagram of this circuit is shown in Fig. 6.3-4, and an SEM photograph of a multiplexer chip is shown in Fig. 6.3-5. The size, excluding probe pads, is only 0.77 mm × 0.54 mm. This circuit utilizes a three stage DFF implemented synchronous counter as an address generator for the multiplexer gate array. The data output of the multiplexer is latched using another DFF stage to prevent glitching. Operation of this multiplexer has been achieved at a clock frequency of 1.1 GHz. Figure 6.3-6 shows the output of the multiplexer at 700 MHz with two inputs biased at V_{DD} and all others at ground. This results in the repetitive

Table 6.3-2

High Speed Performance of DFF Dividers From AR3

Wafer	V_p	Average Clock Freq.	Standard Deviation
AR3-69	1.40 V	1.32 GHz	0.14 GHz (10.6%)
AR3-71	1.07	1.39	0.06 (4.2%)
AR3-79	0.80	0.98	0.14 (14%)
AR3-81	0.76	0.70	0.13 (18%)

bit pattern shown. Figure 6-3-7 shows the output of the multiplexer operating at a clock rate of 1.1 GHz. The power dissipation of the the multiplexer circuits varied from 75 mW to 375 mW for wafers with pinch-off voltages of 0.5 V and 1.45 V, respectively.

A 1 input to 8 output data demultiplexer containing 60 gates was also fabricated and evaluated. The circuit design used for this device is quite similar to the data multiplexer, and could be applied at the receiving end of a high speed gigabit data link. A synchronous counter provides the address for selecting one out of eight NOR gates sharing a common data input. Operation of this circuit has also been demonstrated at a clock frequency of 1.1 GHz. A waveform, measured on a sampling oscilloscope, for an output of the demultiplexer with the input biased at V_{DD} is shown in Fig. 6.3-8. Here operation is shown at clock frequencies of 1.025 GHz and 254 MHz. Bandwidth of the measurement system was limited to 900 MHz by the Tektronix FET probe used to buffer the output of the demultiplexer. The demultiplexer was also evaluated at low clock frequency using a 250 MHz generator as a data source as shown in Fig. 6.3-9. In this figure, both clock input and data output are displayed. An output burst is seen every 8 clock cycles as expected.

8 Stage Shift Register

A SEM photograph of the 8-stage shift register on the AR3 wafers is shown in Fig. 6.3-10 and a block diagram is shown in Fig. 6.3-11. The circuit

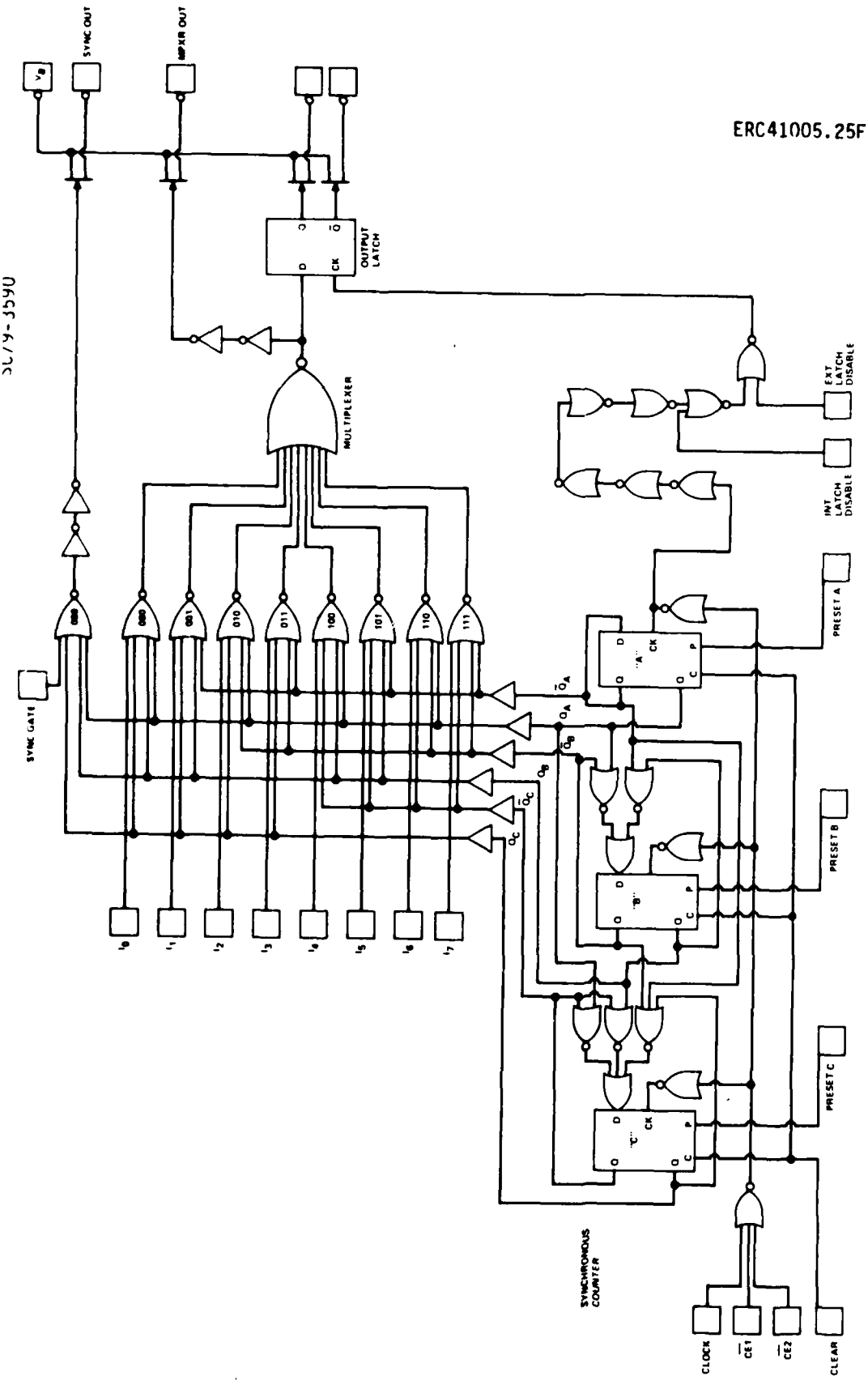

Fig. 6.3-4 Logic diagram of 8 to 1 data multiplexer.

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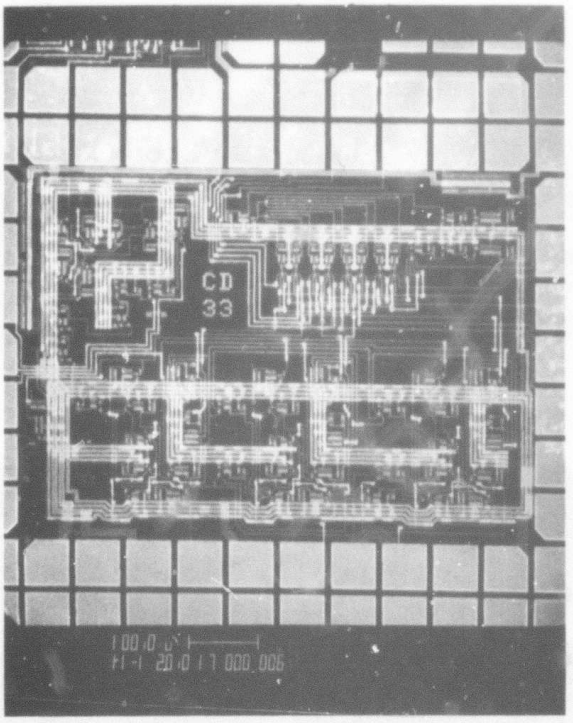
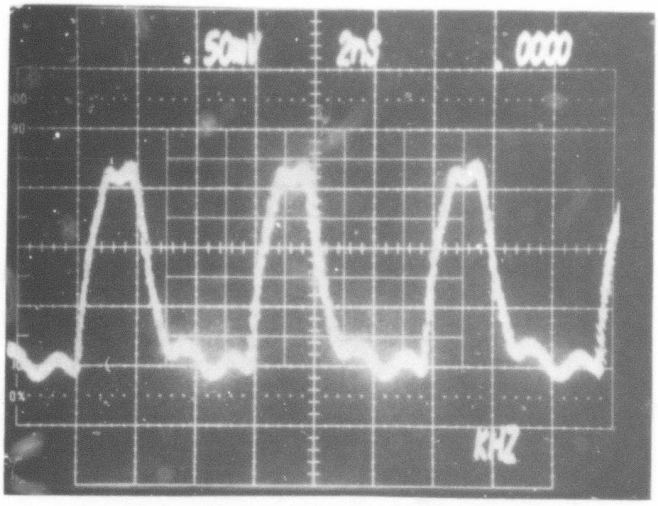


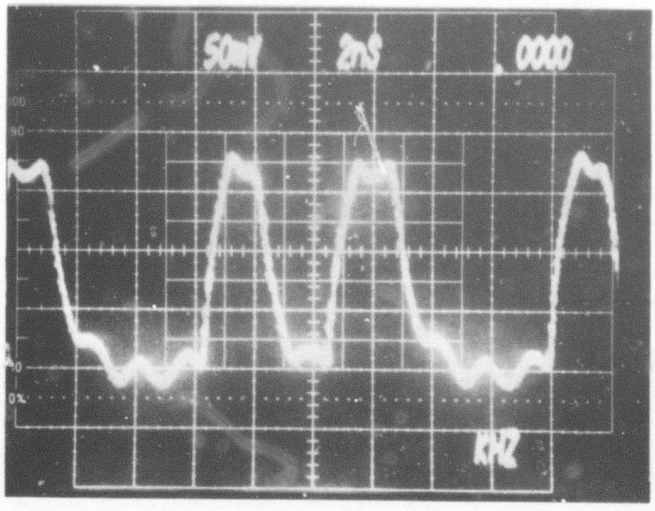
Fig. 6.3-5 SEM photograph of an 8 input data multiplexer containing 64 gates.

MULTIPLEXER OUTPUT
CLOCK FREQ. = 700 MHz

SC79-4391



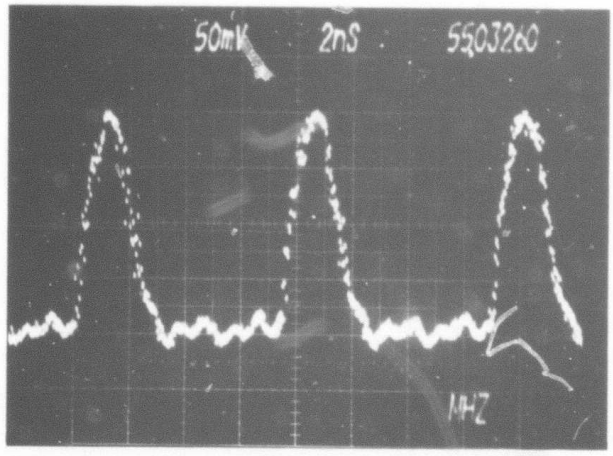
INPUTS 3 AND 7



INPUTS 3 AND 6

Fig. 6.3-6 Multiplexer output with two data inputs selected.

SC79-4060



MULTIPLEXER OUTPUT

0 10 20

NANOSECONDS

CLOCK FREQUENCY = 1.10 GHz

PROPAGATION DELAY = 175 ps/GATE

DYNAMIC SWITCHING ENERGY = 0.85 pJ/GATE

Fig. 6.3-7 Multiplexer output at 1.1 GHz clock frequency.

SC79-4708

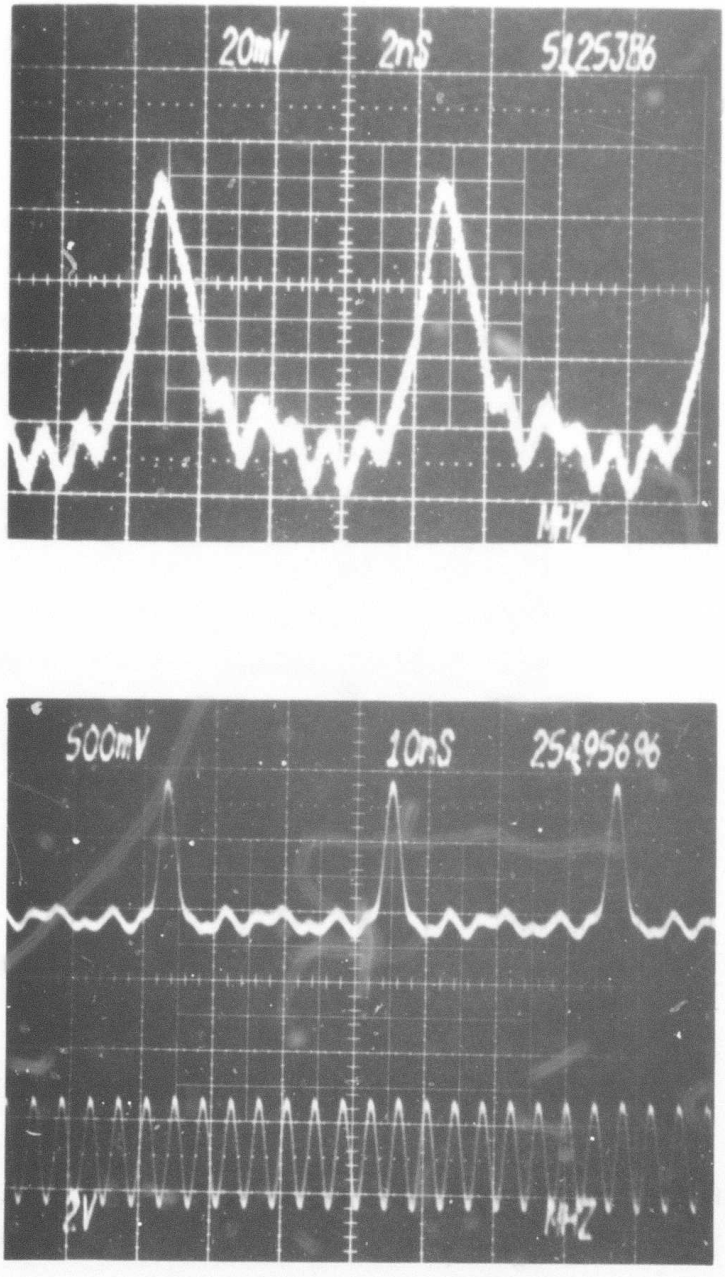
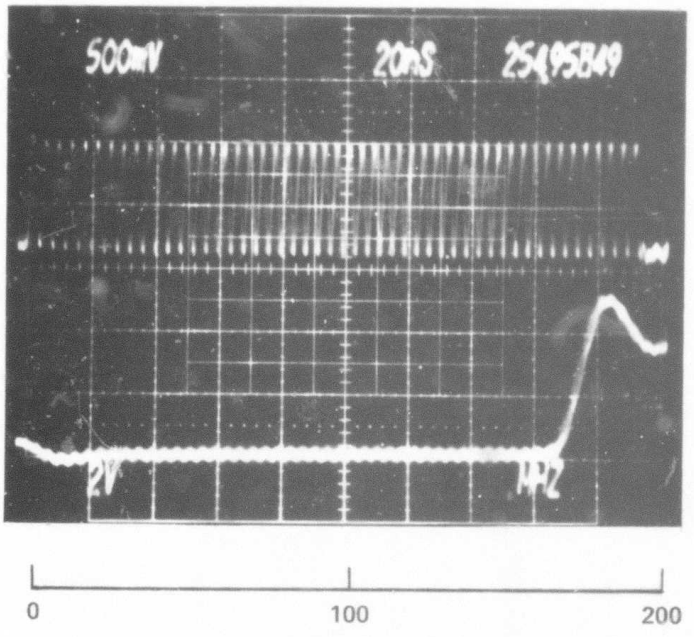


Fig. 6.3-8 Demultiplexer output at 254 MHz (bottom) and 1025 MHz (top) clock frequencies.

SC79-3585



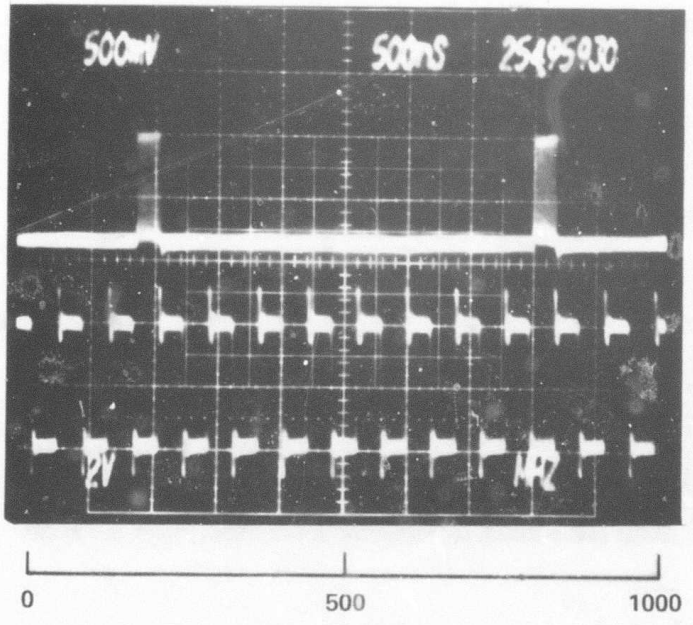


Fig. 6.3-9 Demultiplexer output and clock input with 250 MHz data source. The upper photograph presents an expanded view of the output burst.

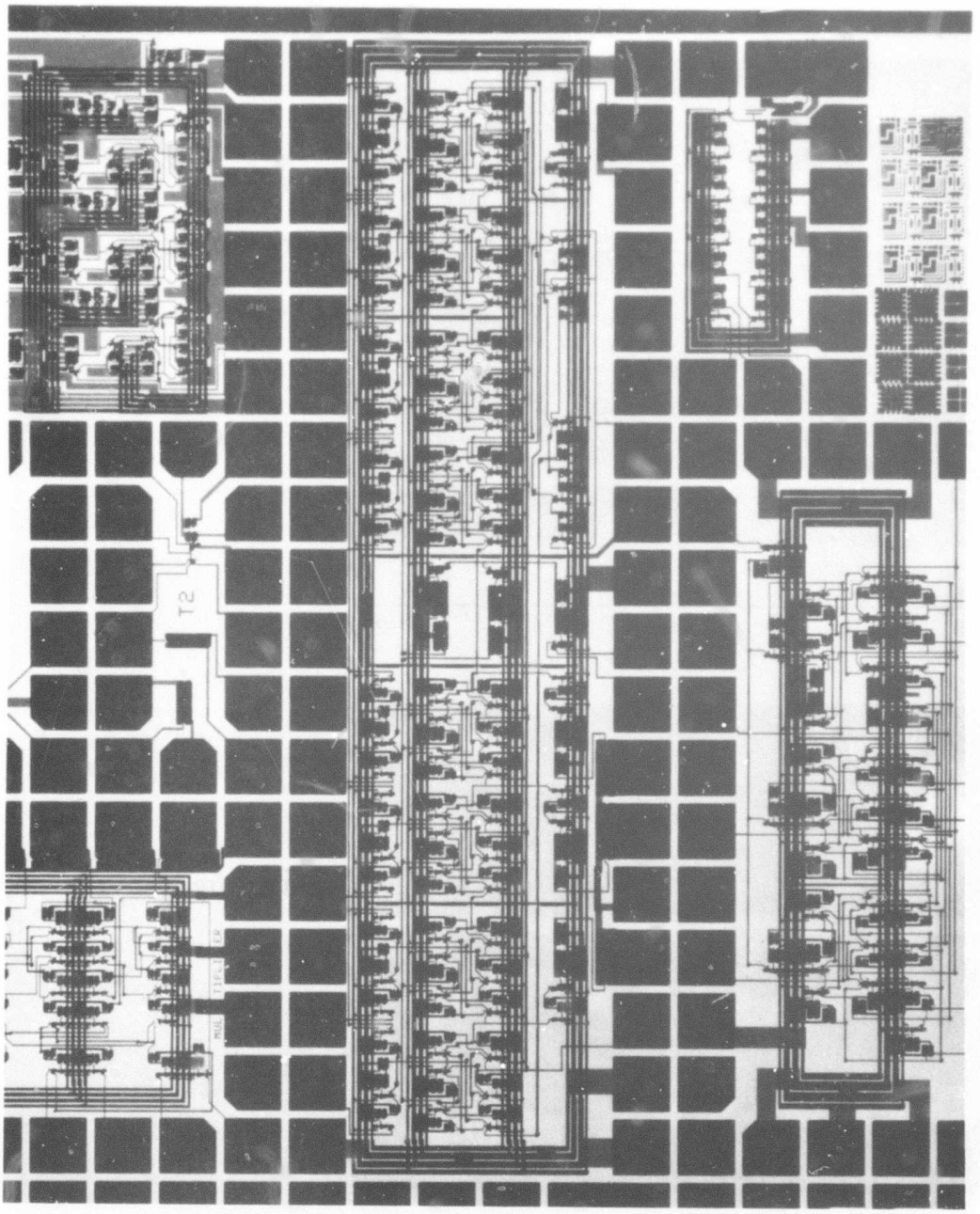


Fig. 6.3-10 Photograph of the 8-stage shift register on mask set AR3.

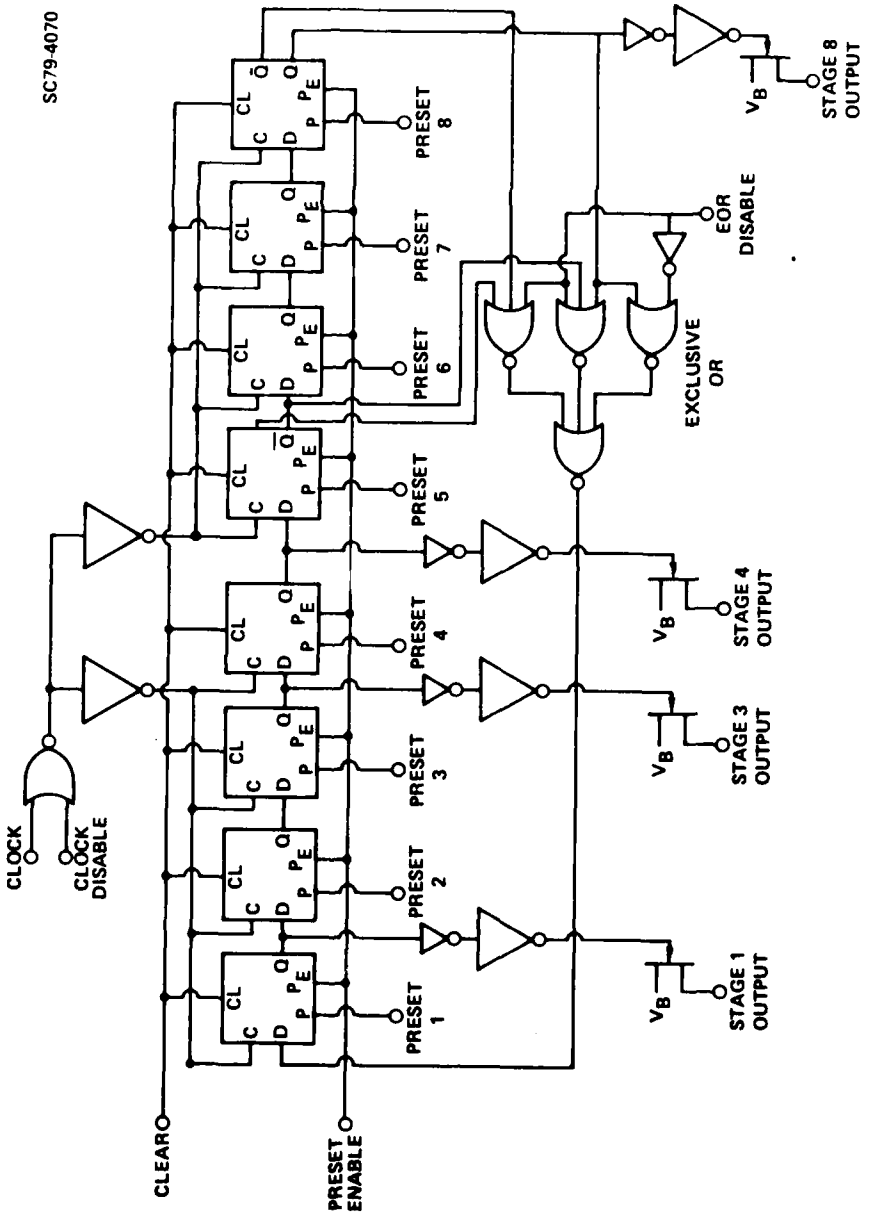


Fig. 6.3-11 Block diagram of the 8-stage shift register on mask set AR3.

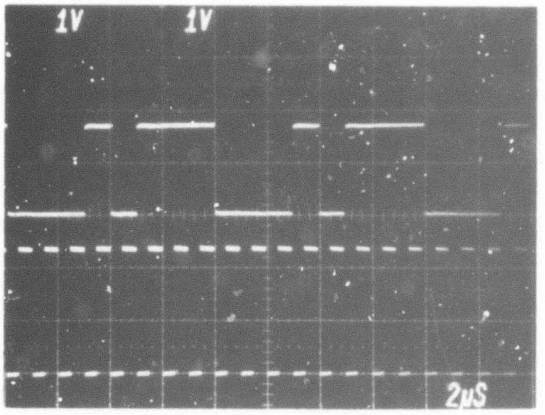
consists of 8 D-type flip-flops (DFF) with a total gate count of 92. The Q output of each stage is connected to the D input of the following stage so that data are loaded into the adjacent flip-flop (and thus "shifted") with each trailing edge of the clock pulse. The Q outputs of the 8th and the 5th stages are also fed into an exclusive-OR (EOR) gate and then connected to the D input of the 1st stage. This exclusive-OR gate is controlled by an EOR line. When it is disabled the output of the 8th DFF feeds back into the first DFF, and the circuit forms a recirculating loop. When the EOR line is enabled the circuit works in the pseudo-noise (P/N) generation mode, which can generate four different patterns depending on the preset inputs of the stages. The 217-bit pattern is generated when stage 1 is preset to "1" and all the other stages are preset to "0." The other patterns are 31-bit and 7-bit long. They can be obtained by presetting the 1st, 2nd, 4th stages and the 2nd, 3rd, 4th, 6th stages to "1," respectively.

The operation of the circuit can be monitored through the buffered outputs of the 1st, 3rd, 4th, and 8th stages. The tests of this circuit were performed with a 36-pin probe card modified to suit the high speed measurement conditions. A preset enable line was connected to a Tektronix PG-502 pulse generator to control the presets of all the stages. A pulse shorter than the clock period was triggered manually to enable all the presets.

Fully working circuits in both recirculation and P/N generation modes have been demonstrated. They are functional at frequencies as high as 350 MHz. The total power dissipation ranged from 50 mW to 120 mW depending on the bias voltages, for wafers with pinch-off voltages from 0.7 to 0.8 V. Figure 6.3-12 shows the output waveforms of a circuit operated in the recirculation mode. Here the circuit was operated at low speed so that the waveforms were not distorted by probe mismatch. The upper trace in Fig. 6.3-12(a) is the output corresponding to a preset pattern of 10111000, and the lower trace is the clock input. The output repeats itself every 8 clock cycles, and changes state on the trailing edge of the clock pulse. Figure 6.3-12(b) is the photograph of an output corresponding to 11100000 presetting with a clock frequency of 352 MHz.

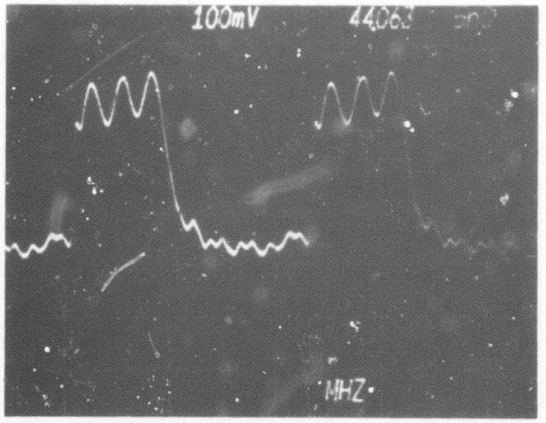
SC79-6393

(a)



RECIRCULATION
PATTERN
10111000

(b)



RECIRCULATION
PATTERN
11100000

f_c = 352 MHz

P_D = 1.27 mW/gate

Fig. 6.3-12 Waveform for the 8-stage shift register operating in the recirculation mode. (a) Low speed waveforms showing the output (upper trace) and the clock (lower trace); (b) high speed output.

The maximum clock rate at which the shift register was able to operate (350 MHz) was low, and yet the circuit is employing the same D-flip-flop buidling blocks used for ÷8 circuits on mask sets AR2 and AR3. The dividers operated at frequencies as high as 1.9 GHz. The cause for the low speed of the shift register was traced to a design error. The 8th stage of the divider and the EOR gate output (see Fig. 6.3-11) were not provided with buffers to drive the relatively large capacitive load of the long return lines. This error was corrected int he design of the larger shift register for the new mask set AR4.

The P/N generation operation is demonstrated in Fig. 6.3-13. Here Figures (a), (b), and (c) correspond to three different patterns, 7-bit, 31-bit, and 217-bit long, respectively. The upper trace in each picture is the output waveform and the lower trace the frequency spectrum of the output. The spacing between the adjacent spikes in each spectrum is the fundamental frequency of the operation. It equals f_c/n, where f_c is the clock frequency, and n is 7, 31, or 217 depending on the mode of operation. It can be seen clearly in the pictures that the wave pattern repeats itself every 7 clock cycles in Fig. 6.3-13(a) and every 31 clock cycles in Fig. 6.3-13(b). Part of the wave pattern of the 217-bit mode is shown in Fig. 6.3-13(c). The spectrum indicates that it operates in the correct mode.

The measured frequency spectra have been compared with the theoretical spectra calculated from Fourier analysis. The comparison is shown in Fig. 6.3-14 with the calculated values indicated by dots and the measured values by crosses. The 7-bit mode measurement was made at a clock frequency of 140 MHz, and the 31-bit mode at 100 MHz. As the figure shows, the measured spectral amplitudes agree very well with the calculated amplitudes except for the point at the clock frequency. The large harmonic at the clock frequency is due to the clock feed-through which is apparent on the waveforms shown in Fig. 6.3-13.

In conclusion, the GaAs 8-stage shift register with almost 100 gates has been successfully fabricated and evaluated. The circuit worked in both recirculation and P/N generation modes as expected. These results have been very useful for the design of the larger (64-stage, 550 gates) shift rgister incorporated in mask set AR4.

SC79-7166

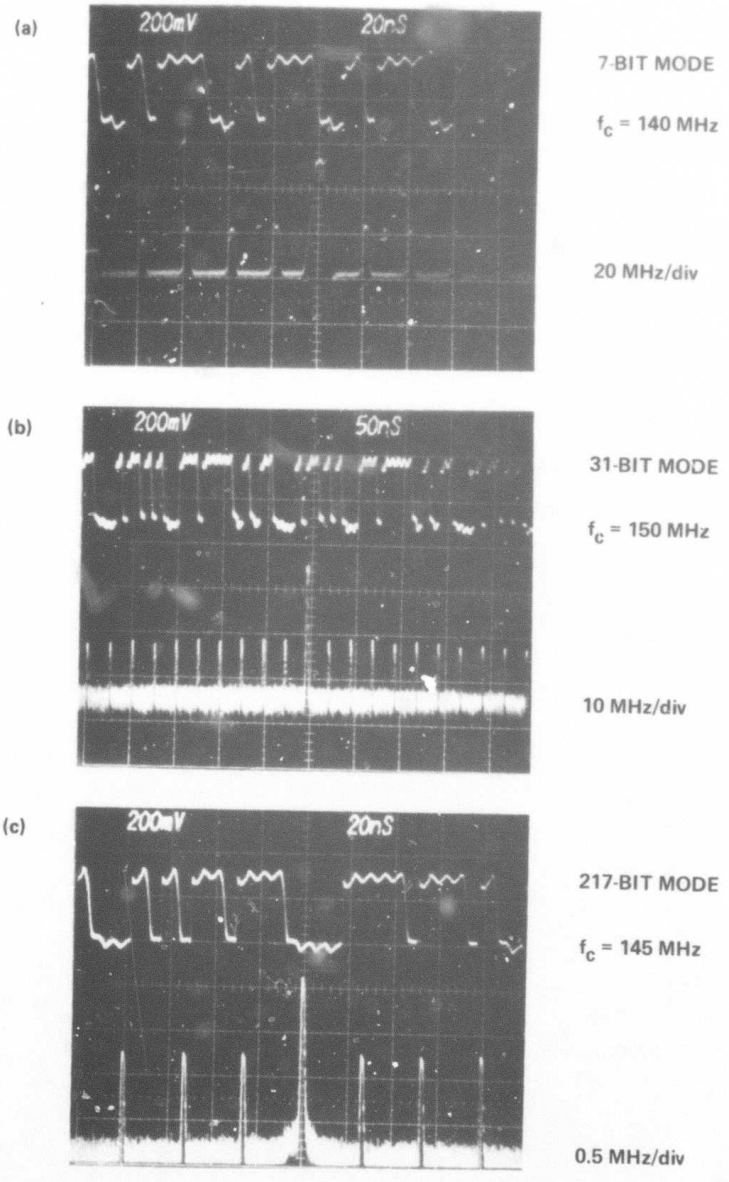


Fig. 6.3-13 Output waveforms for the 8-stage shift register operating in the pseudo-noise generation mode. The upper traces represent the output for each of the three codes while the lower traces represent the corresponding frequency spectra.

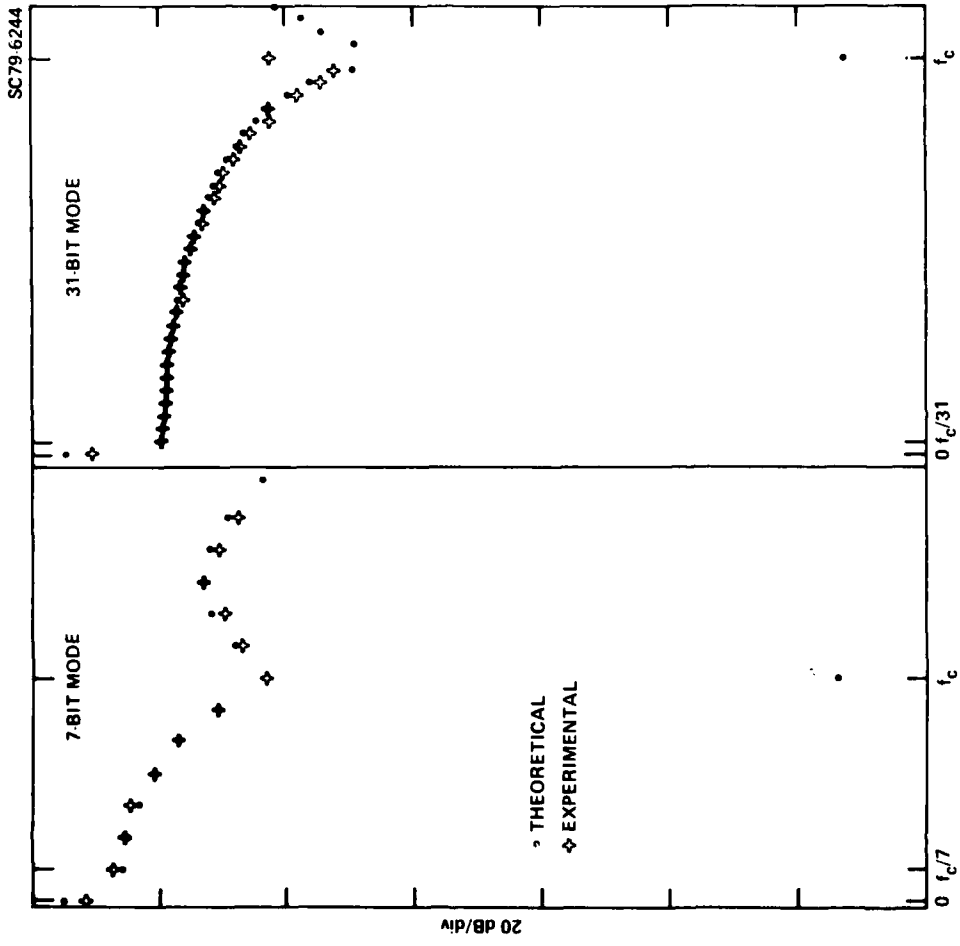


Fig. 6.3-14 Theoretical and experimental frequency spectra for the output of the 8-stage shift register operating in the P/N mode.

2 × 32 Stage Shift Register

A photograph of the 2 × 32 stage shift register located on maks set AR4 is shown in Fig. 6.3-15, and a block diagram is shown in Fig. 6.3-16. The circuit consists of 64 D-type flip-flops (DFF) with a total gate count of 550. As in the 8-stage DFF, the Q output of each stage is connected to the D input of the following stage, so that data are loaded into the adjacent flip-flop (and thus "shifted") with each trailing edge of the clock pulse. The operation of the shift register circuit can be monitored through the buffered output of the 1st, 2nd, 13th, 18th, 28th, 33rd, 34th, 45th, 50th and 60th stages.

A control circuit which consists of 24 NOR gates and three control input lines, is implemented for the control of the operation modes of the 64-stage shift register. A logic diagram of the control circuit is given in Fig. 6.3-17. The five possible operation modes and their required control input conditions are given in the table below the schematic. Control line #1 is designed to enable the serial cascading of the two sets of 32-stage shift registers (to form a 64 stage shift register), control line #2 to disable the operation of P/N generator, and control line #3 activates the serial data in/serial data out operation.

The evaluation of the shift register circuit has been carried out. Partially functional shift registers with more than 60 (out of the 64) registers operational have been found. The operation of this device is illustrated in Fig. 6.3-18. The devices operated in the serial loading mode where a negative going pulse is fed into the serial data input of the 1st stage DFF for every 64 clock cycles. The clock driver input to the shift register is shwon as the top oscilloscope trace in the upper photograph in Fig. 6.3-18. Below the clock trace is shown the inverted output of the 1st stage. The output from Q_{33} is shown as the bottom trace.

The lower photograph in Fig. 6.3-18 shows that the shift register functioned in the 1 × 64 serial loading mode up through stage 60. This photograph also illustrates one of the problems observed in operating this circuit, the problem of data loss or gain. Data tended to be lost or gained

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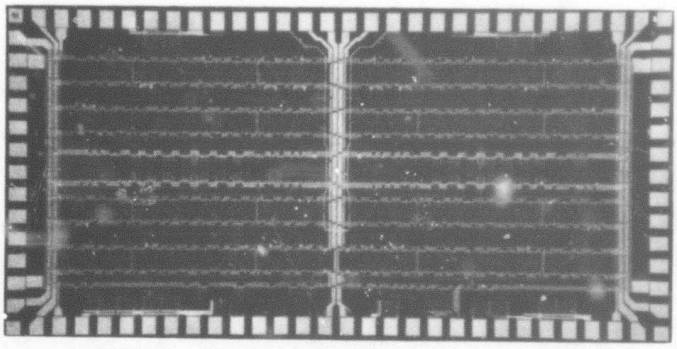

Fig. 6.3-15 Photograph of the 2 × 32-stage shift register fabricated from mask set AR4. This circuit has 550 gates.

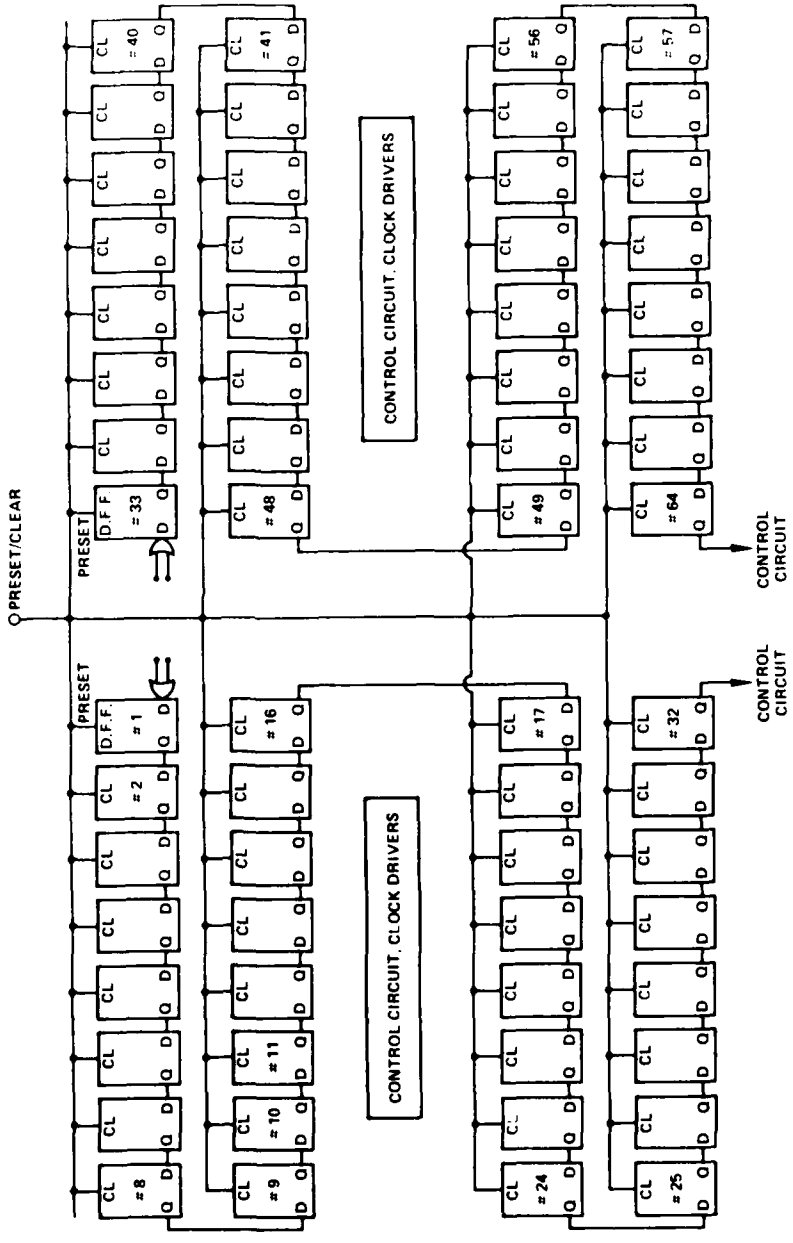

Fig. 6.3-16 Block diagram of the 64-stage shift register on mask set AR4.

SC79-6341

AR-4 2 x 32 BIT SHIFT REGISTER CONTROL CIRCUIT DIAGRAM

CONTROL #1 ENABLE 1 x 64
CONTROL #2 DIABLE PATTERN GENERATOR
CONTROL #3 ENABLE SERIAL DATA IN

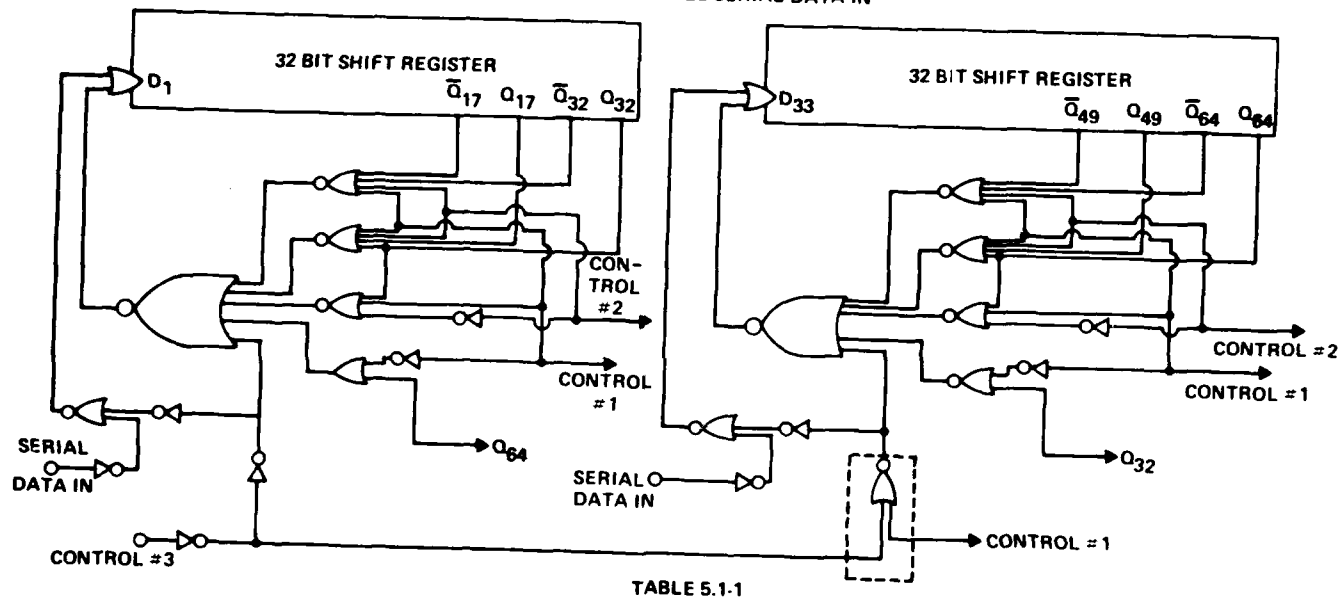

TABLE 5.1-1

	CONTROL #1	#2	#3	
A	0	1	0	2 x 32 RECIRCULATE
B	0	X	1	2 x 32 SERIAL DATA IN, SERIAL DATA OUT
C	1	X	1	1 x 64 SERIAL DATA IN, SERIAL DATA OUT
D	1	X	0	1 x 64 RECIRCULATE
E	0	0	0	2 x 32 PATTERN GENERATOR

Fig. 6.3-17 Logic diagram of the control circuit for the 64-stage shift register on mask set AR4.

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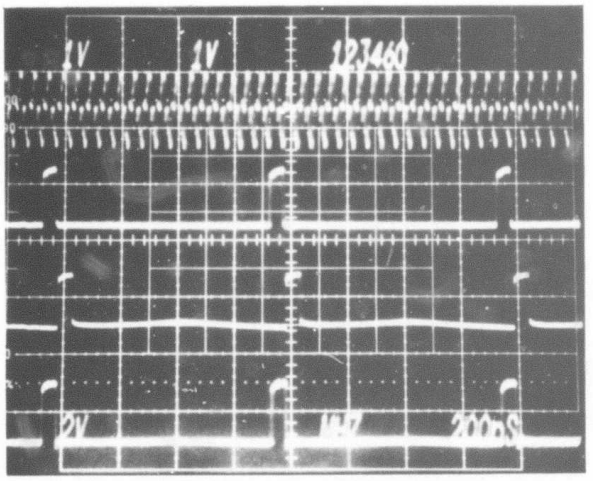

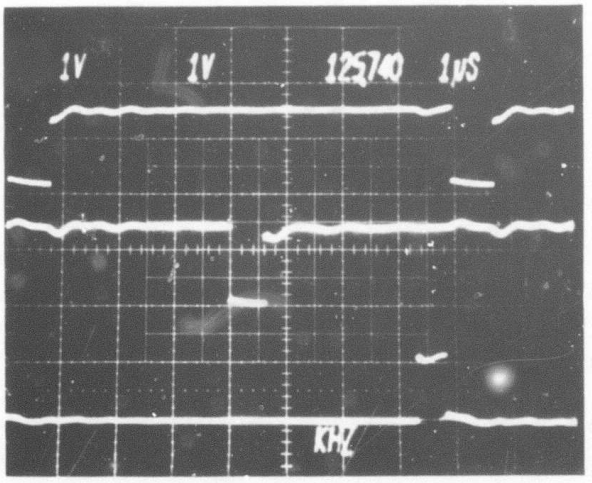

SERIAL DATA IN = 1/64 f_{CLOCK}

Fig. 6.3-18 Clock input and data output measured on the 64 stage shift register circuit. Data shifting up through stage 60 in the serial load mode is demonstrated in the lower photograh.

during the shifting operation such that it was necessary to serial load data pulses two or three clock cycles wide in order to obtain an output at stage 60. Another associated symptom was the failure to operate in a recirculation or P/N code generation mode, both of which require accurate data transfer to avoid latch up of the register.

These problems were not anticipated because of the very well established and successful performance of SDFL D Flip-Flops in many of the circuits discussed above. However, on further examination, it became evident that large synchronous high speed circuits such as this LSI shift register present some rather severe mesurement problems in comparison to theire smaller SSI or MSI counterparts. First of all, all measurements have been performed at wafer probe using commercially available probe cards with 2 to 2.5 cm probes. These probes contribute a significant series inductance (approximately 30 nH) on all supply and ground connections. On large synchronous circuits where many gates are switching at high speeds on the same clock edges, large supply and ground current transients lead to supply voltage spikes or dropouts which could easily result in a momentary data loss in a latch circuit. Thus, improvements in the test conditions are clearly needed, either by packaging devices in low inductance packages or by reduction in probe inductances. In addition, further improvements are indicated in the IC layout in order to minimize voltage spikes due to current transients induced by large clock buffer gates. More extensive on-chip bypass capacitors and separate ground returns for clock buffers would probably help protect critical latches from data loss due to ground transients.

Summary

In Section 6.3, the design and operation of MSI and LSI sequential circuits was described. These circuits were all designed as demonstration circuits for this technology development program. Many of these circuits were shown to be totally functional and operational at high speeds with good yields being observed on the more widely characterized ripple divider circuits. Directions for future circuit design and test methodology improvements have also been established by the thorough characterization of the more demanding synchronous cir-

cuits where critical timing paths and current transient effects are much more evident.

6.4 Parallel Multiplier Circuits

A particularly attractive candidate for a representative combinatorial logic circuit is a parallel multiplier, since multiplication frequently represents a bottleneck in signal processing and computer systems. Typical sizes for a high-speed parallel multiplier would be 8 x 8 bits or 16 x 16 bits, with larger products formed of combinations of these. A straight parallel multiplier, N x N bits, without carry lookahead and not using more complex (e.g., Wallace tree) approaches, requires N(N-2) full adders and N half adders in its implementation and requires a total of (N-1) sum delays plus (N-1) carry delays to obtain the product. A goal of the current GaAs IC program was to construct an ~1000 gate 8 x 8 parallel multiplier chip (700 gates multiplier plus I-O latching and buffering). This goal was met by designing, fabricating and testing parallel multipliers of 3 × 3, 5 × 5 and 8 × 8 bits.

Since the bulk of a large multiplier is full adder cells, the speed of these cells dictates the multiply time. Figure 6.4-1 shows the logic diagram for a NOR-implemented full adder cell. By using a full minterm expansion for both sum and carry, the propagation delays are kept to $2\tau_d$ for the carry and 3 τ_d for the sum (where τ_d is the NOR gate delay). A total of 12 gates (9 NORs and 3 inverters) are required per full adder cell.

3 × 3 Parallel Multiplier

As a first step toward the realization of an 8 × 8 bit LSI high performance GaAs multiplier chip, a 3 × 3 bit circuit was designed and included on mask set AR3. This MSI circuit, with a gate count of 75, was fabricated using the planar SDFL approach. Figure 6.4-2 shows a logic diagram for the 3 × 3 multiplier chip were "F" represents a full adder (12 gate) cell and "H" represents a half-adder (5 gate) cell. Figure 6.4-3 shows an SEM photograph of this circuit which measures only 0.54 × 0.77 mm (excluding probe pads).

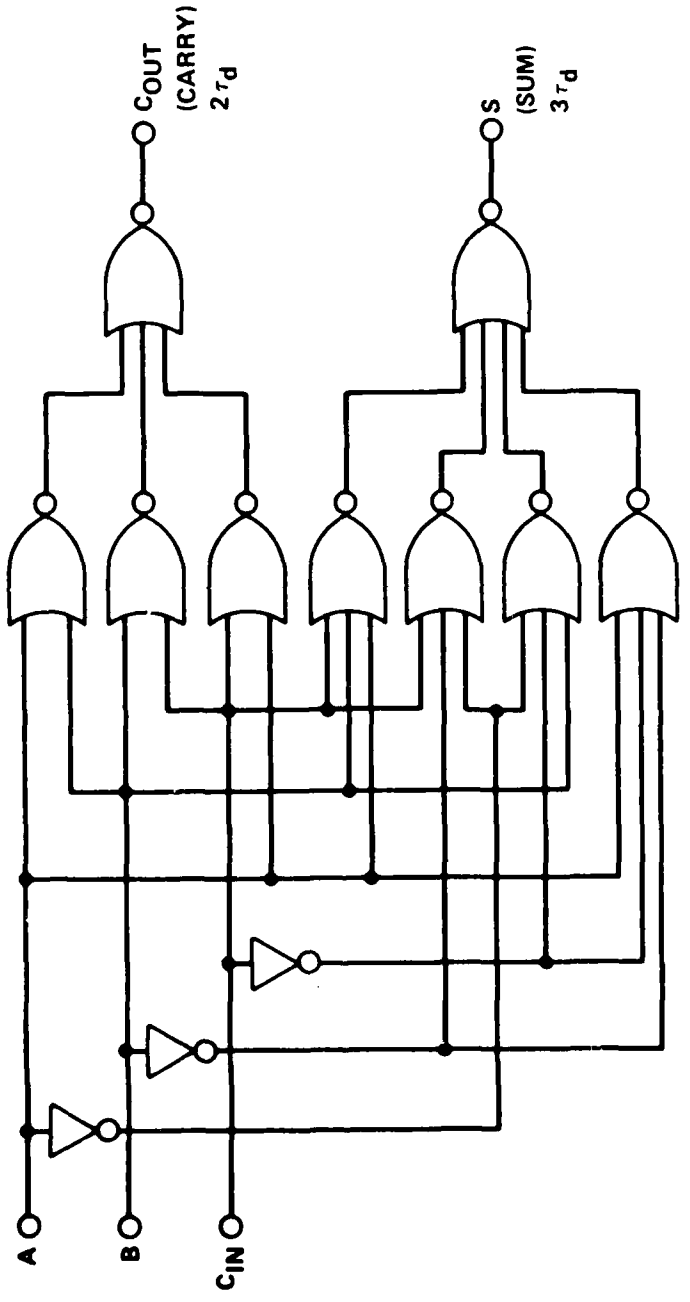

Fig. 6.4-1 Logic diagram of a NOR-implemented full adder cell.

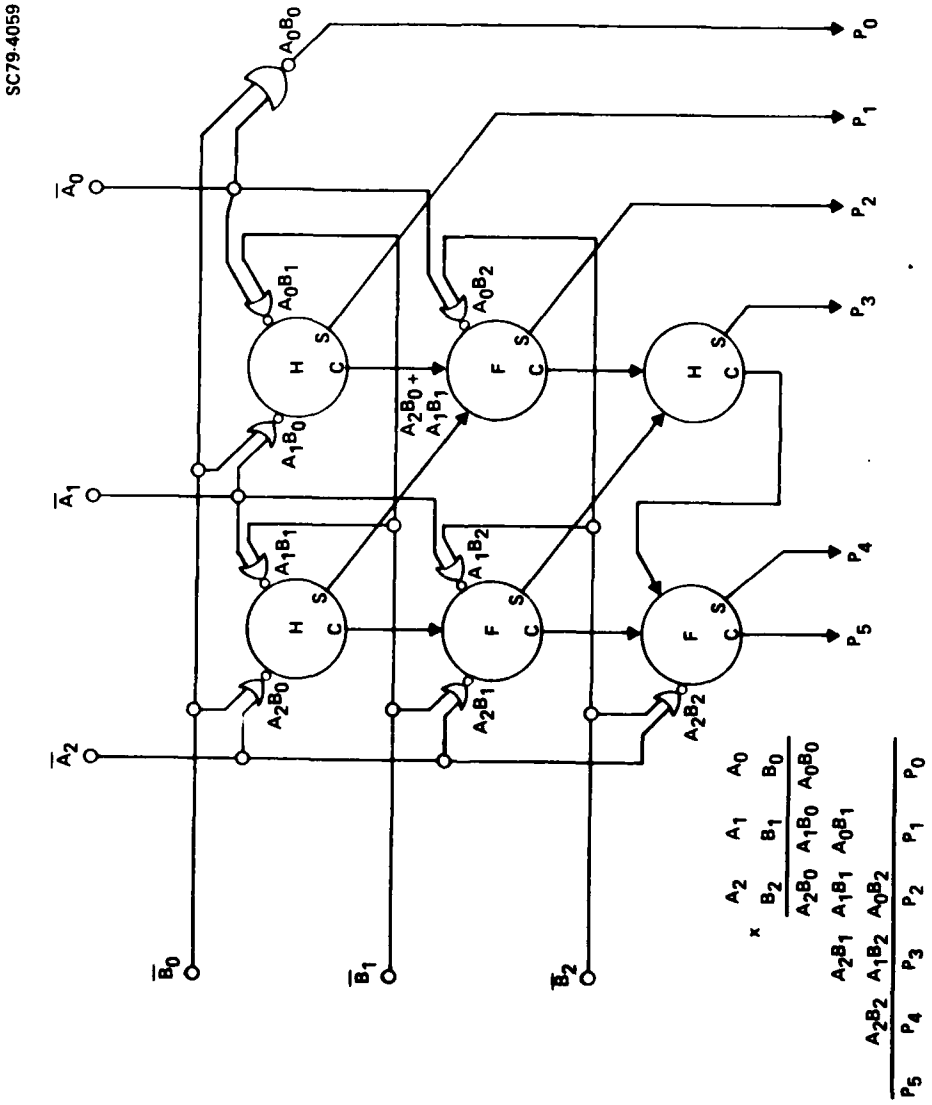

Fig. 6.4-2 Block diagram of the 3 × 3 bit parallel multiplier on.

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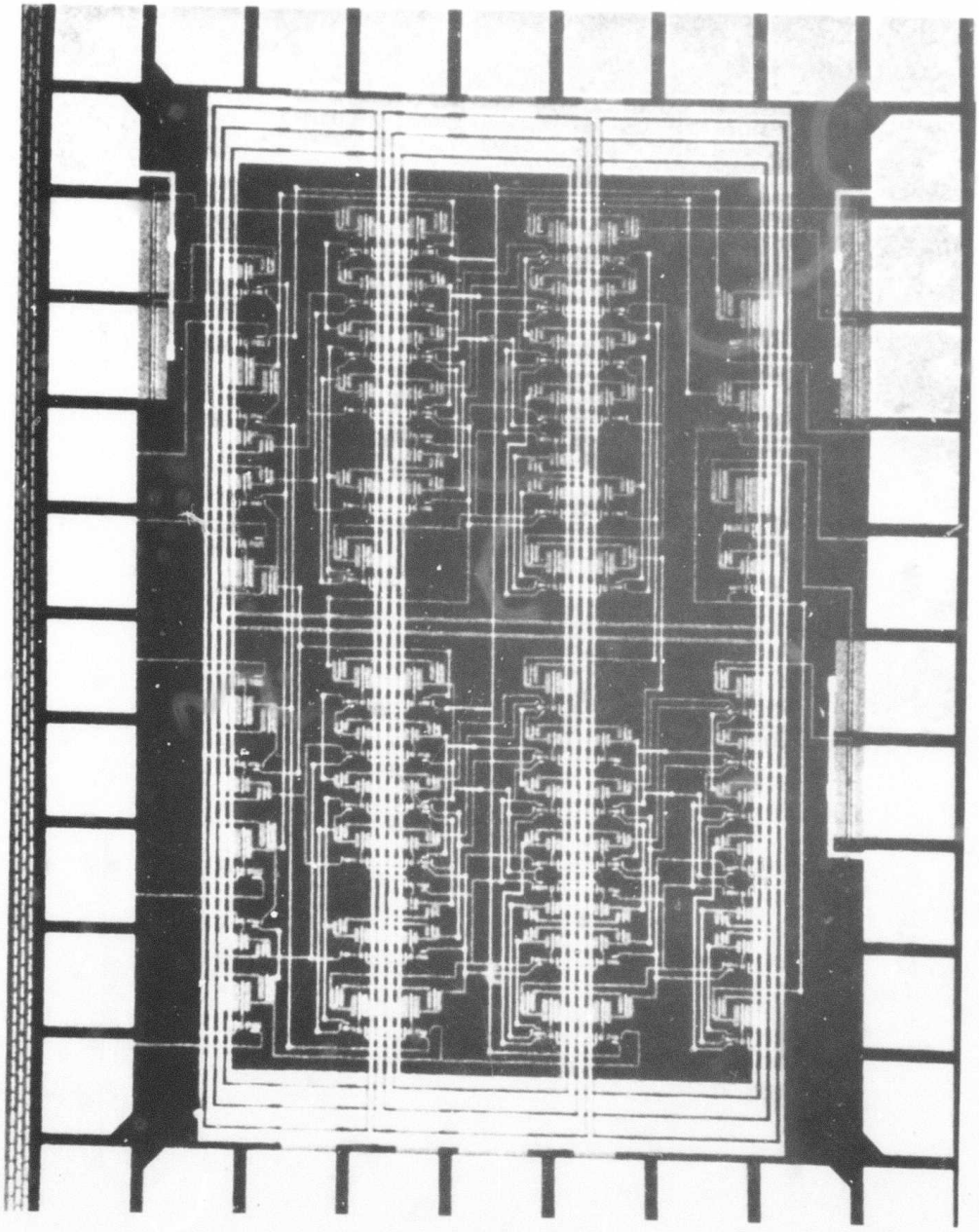


Fig. 6.4-3 SEM photograph of the 3 × 3 bit parallel multiplier.

The 3 x 3 bit multiplier has been evaluated for both logic functionality (at low speed) and high speed operation. To perform a complete low speed functionality test, all 64 input combinations ($2^3 \times 2^3$) should be exercised. Each of the six output bits must be inspected for each input combination. Thus it becomes impractical to thoroughly evaluate the multiplier manually, without computer aided test capability. Automatic testing becomes mandatory for the larger (5 x 5 and 8 x 8) multipliers. A MACSYM II (Analog Devices) automatic data acquisition system has been installed and used in conjunction with an Electroglas wafer probe station to perform the automatic testing of the multiplier. The data acquisition system contains a 16-bit microcomputer with dual disk storage and digital as well as analog I/O capability. Software and hardware were developed so that the performance of the multiplier chip could be evaluated for all 64 possible input combinations. Figure 6.4-4 shows a block diagram of the test setup using the MACSYM II system. All product outputs are monitored and stored on disk by the MACSYM. The output voltage levels are decoded into logic states and compared with the results of the calculated binary multiplications for the specific input states. If the results do not match, error codes are generated. The circuit was found to operate correctly for all possible combinations of input bits.[38,39]

More insight into the operation of the 3 x 3 bit multiplier (at low speed) can be gained by looking at some outputs through an oscilloscope. Input codes 111 x 10S = S$\bar{S}\bar{S}\bar{S}$SS were chosen to demonstrate the correct functions. S stands for a square-wave signal applied to the A_0 input while all the other inputs are fixed (with ground = logical "0" and V_{DD} = logical "1"). The S input corresponds to the upper trace in Fig. 6.4-5 Upon this A_0 pulse input, the product outputs P_2, P_3, and P_4 display the inversion of S, and the other outputs assume the waveform of A_0. The traces for all six outputs are displayed in Fig. 6.4-5 showing proper operation. The total power dissipation for the 3 x 3 multiplier of Fig 6.4-5 was 31.5 mW with V_{DD} = 1.77 V and V_{SS} = -0.94 V, corresponding to a power dissipation of 420 μW per gate.

To evaluate the multiply time or gate propagation delay in the cells, an optional NOR control gate and a feedback loop from P_5 (the most significant

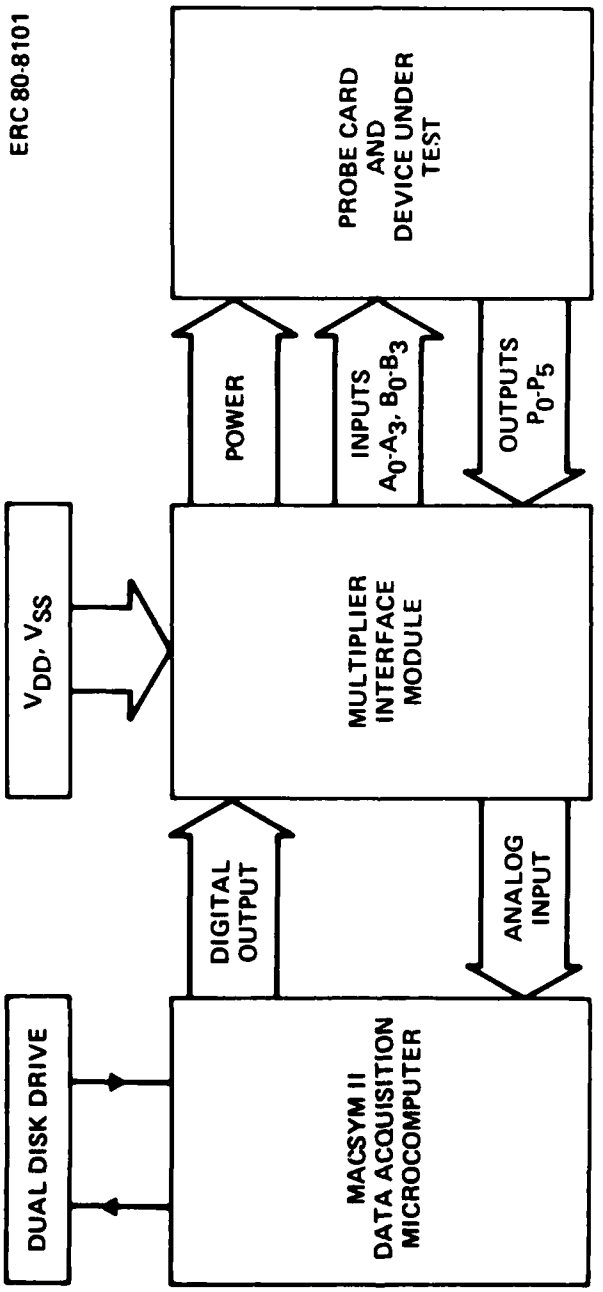


Fig. 6.4-4 Block diagram of the test setup using the MACSYM II data acquisition system.

SC79-5648

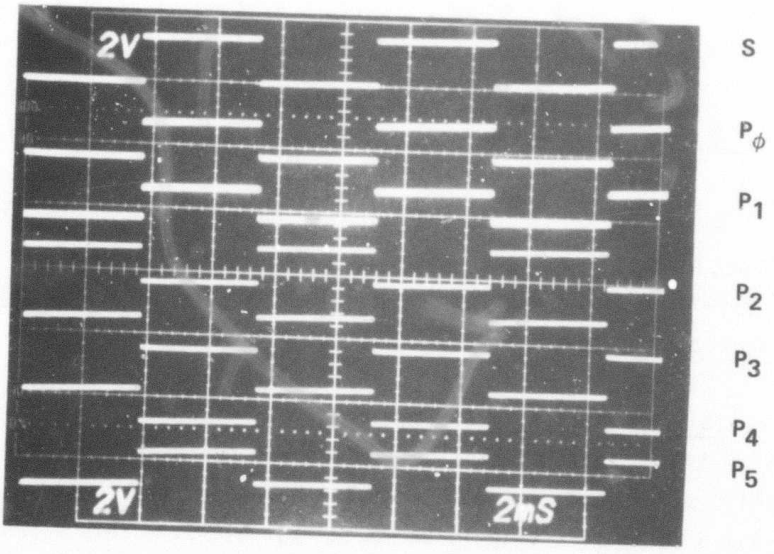


Fig. 6.4-5 Outputs from the 3 × 3 bit parallel multiplier when the inputs are 111 and 10S, where S is the square wave displayed as the upper trace.

bit of the product) to A_0 (the least significant bit of the multiplicand) was included to allow operation of the multiplier in a feedback mode. This approach is illustrated by Fig. 6.4-6. The on-chip feedback causes the multiplier to oscillate with a period determined by the total delay through the A_0 - P_5 path which corresponds to 3 full adder carry delays ($6\tau_d$) plus 3 NOR gate delays for a total of $9\tau_d$. Therefore, the oscillation frequency will be $f_0 = 1/18\tau_d$. This testing approach eliminates the requirement for a very fast pulse to be delivered to an input and for a very short delay time to be accurately measured from input to output. Instead of this, a self-oscillation frequency can be measured easily off chip and accurately related to the multiplier delay time.

Evaluation of the 3 x 3 multiplier in this mode was performed, and an oscillation frequency of 323 MHz, as shown in Fig. 6.4-7, corresponding to τ_d = 172 ps was obtained at V_{DD} = 2.28 V, and V_{SS} = -0.79 V. The power dissipation was P = 56 mW (P_C = 750 μW/gate), corresponding to $P_D\tau_d$ = 129 fJ. Multipliers on lower pinch-off voltage wafers operated at f_0 = 246 MHz, corresponding to τ_D = 225 ps with a power dissipation P = 31.5 mW (420 μW/gate) for $P_D\tau_d$ = 95 fJ. This corresponds to a 3 bit multiplication time of about 1.5 ns.

5 × 5 Parallel Multiplier

A 5 x 5 bit parallel multiplier was designed and incorporated on mask set AR4. Wafers containing this device have been fabricated. A photomicrograph of a 5 x 5 multiplier chip is shown in Fig. 6.4-8. This circuit has a total gate count of 260. The operations required to multiply two 5-bit binary numbers ($B_4B_3B_2B_1B_0 \times A_4A_3A_2A_1A_0 = P_9P_8P_7P_6P_5P_4P_3P_2P_1P_0$) are illustrated in Fig. 6.4-9. The addition of the partial product terms a_ib_j required to perform the multiplication is accomplished by properly combining full adders (FA) and half adders (HA) as shown in Fig. 6.4-9. Five half adders and fifteen full adders are used.

Two NOR control gates and a feedback path from P_9 (the most significant bit of the product) to B_0 (the least significant bit of multiplier) have been added as in the 3 × 3 multiplier to provide a high speed feedback operating mode to assist in high speed evaluation. By presetting the multiplicand $B_4B_3B_2B_1B_0$ to 10000, the multiplicand $A_4A_3A_2A_1A_0$ to 11111, and setting the feedback enable

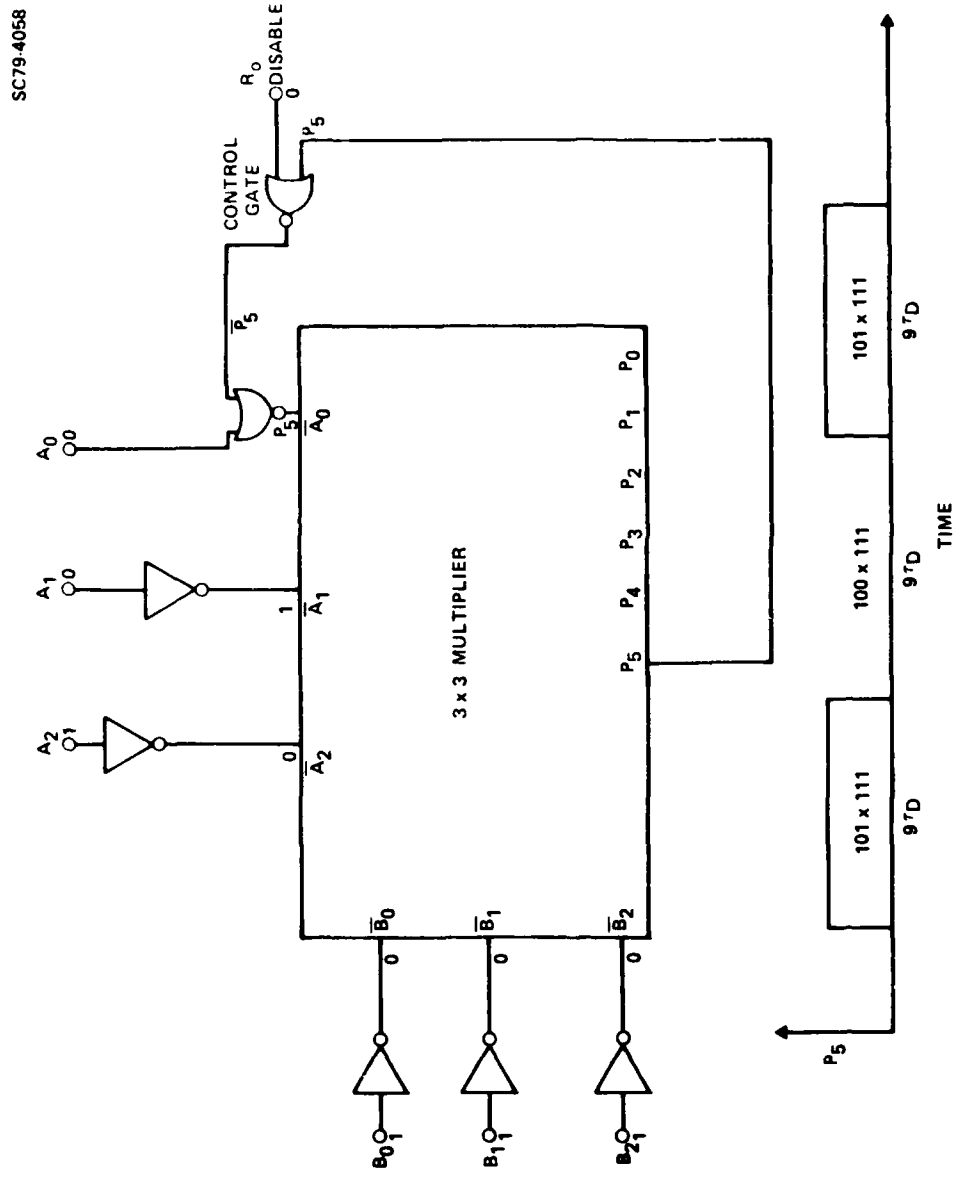
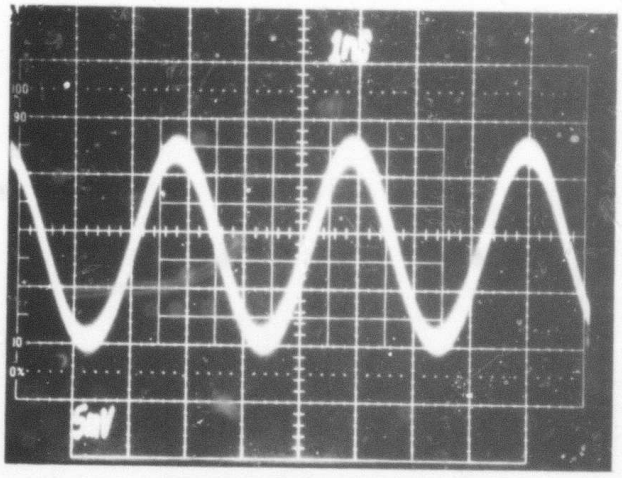


Fig. 6.4-6 Block diagram of the overall 3 × 3 multiplier circuit showing the feedback mode used for high-speed testing.

SC79-6497



V_{dd} = 2.3V f = 323 MHz (τ_d = 172 ps)

V_{ss} = -0.8V P_D = 750 μW/GATE

$P_D\tau_d$ = 128 fJ

LOWEST POWER $P_D\tau_d$ = 94.5 fJ

τ_d = 225 ps

Fig. 6.4-7 Highest operating speed of the 3 × 3 bit parallel multiplier operated in the "ring oscillator mode." Speed and power dissipation figures are displayed.

SC80-7680

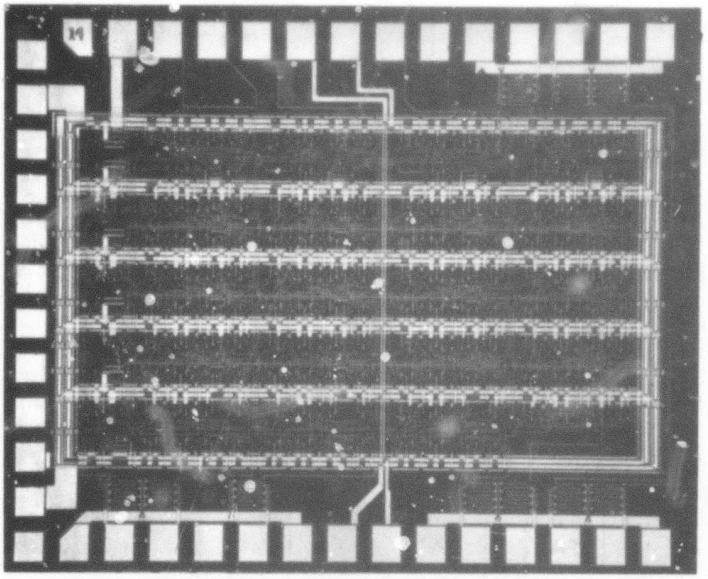


Fig. 6.4-8 SEM photograph of the 5 × 5 bit parallel multiplier on mask set AR4.

SC79-6265

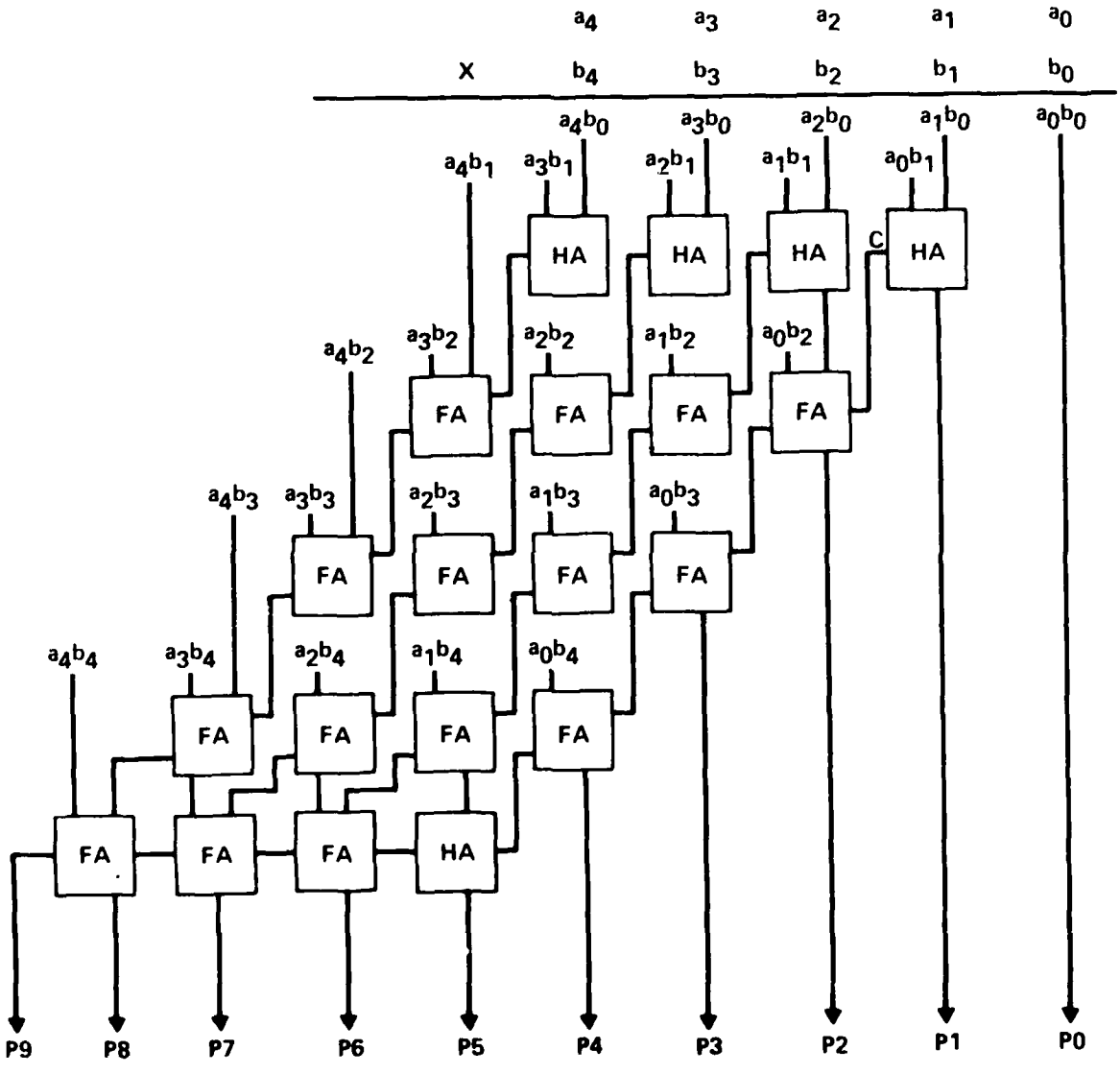


Fig. 6.4-9 Logic diagram of the 5 × 5 bit parallel multiplier on mask set AR.

control to "high", the multiplier will oscillate in the feedback mode. An oscillation frequency of $1/44\tau_d$ is expected. To ease the presetting of inputs A and B, an optional common input line (feedback mode preset) is connected to the A_0, A_1, A_2, A_3, A_4 and B_4 input NOR gates, so that all these inputs can be preset simultaneously through the common input line. With the feedback enable control gate set to "low", the data of P_9 will not be able to feed to B_0 through the feedback loop, so that the normal multiplier operation will be resumed.

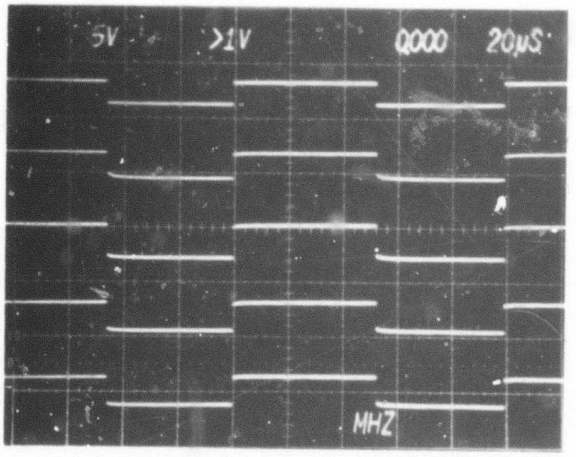
Evaluation of the 5 × 5 parallel multiplier chips was carried out at wafer probe following the procedures described in the discussion of the 3 × 3 multiplier. Functionality evaluation was carried out at low speeds using the MACSYM II automatic data acquisition system. All 1024 possible input combinations were exercised and the ten output bit states were read as analog signals and decoded for each test condition. This circuit was verified by this technique to be fully functional for all test combinations. Wafer yields as high as 15% have been observed to date on this 260 gate LSI circuit.

Ripple testing of the multiplier has also been performed by applying a pulse input to b_0 and performing the product shown in the inset in Fig. 6.4-10 by use of the feedback mode preset line. Here, b_0 and inversion of b_0 are seen at all outputs as required by the 31 × 16 product. For the chip shown in Fig. 6.4-10, the power dissipation was only 155 mW or 596 μW/gate. Power dissipation as low as 420 μW/gate has also been observed on fully functional 5 × 5 parallel multiplier chips.

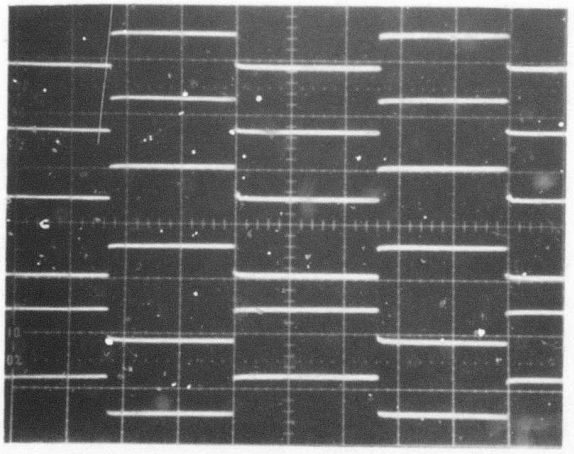
High speed evaluation has also been performed on the 5 × 5 multiplier circuits by use of the P_9 to b_0 on-chip feedback path described above. Operation in this mode is illustrated by Fig. 6.4-11. In the top photograph of this figure, the feedback oscillations are shown as gated by a pulse applied to the b_0 input. Since the b_0 input is a 2 input NOR gate with one input from off-chip and one input from the inversion of P_9, a high b_0 input will also disable the feedback. This demonstrates that the oscillations observed are the intended ones and not some spurious parasitic oscillation. The lower photograph of Fig. 6.4-11 is an expanded view of the oscillation, in this case at 109.1 MHz.

ERC80-9698

RIPPLE TEST (31 x 16)



b_0
P_0
P_1
P_2
P_3



P_4
P_5
P_6
P_7
P_8
P_9

$$\begin{array}{r} 1\ 1\ 1\ 1\ 1 \\ 1\ 0\ 0\ 0\ b_0 \\ \hline b_0\ b_0\ b_0\ b_0\ b_0 \\ 1\ 1\ 1\ 1\ 1 \\ \hline b_0\ b_0\ b_0\ b_0\ b_0\ b_0\ b_0\ b_0\ b_0\ b_0 \end{array}$$

P_D = 155 mW (596 μW/GATE)

V_{DD} = 2.0V

V_{SS} = -1.2V

Fig. 6.4-10 5 x 5 parallel multiplier performance under ripple test conditions. A pulse was applied to the b_0 input (top trace) and each product bit examined as the product 31 x 16 was exercised.

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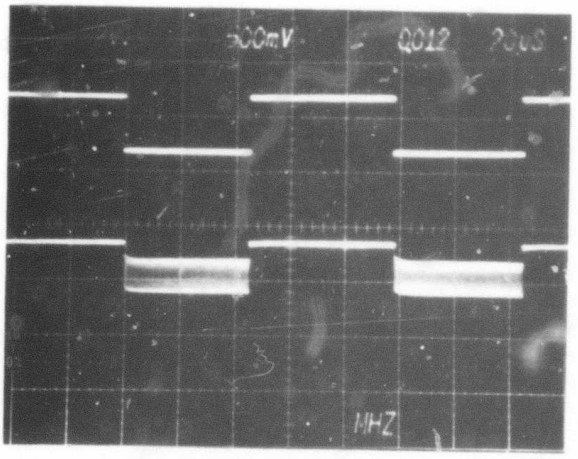
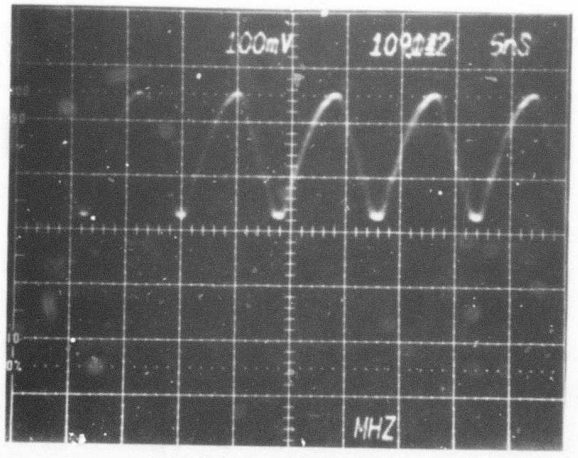


b_0

P_{15}



P_{15}

FEEDBACK MODE

P_D = 183 mW (703 μW/GATE) f_{OSC} = 109.1 MHz = 1/44 τ_d

τ_D = 208 ps (190 ps WHEN CORRECTED FOR FEEDBACK PATH DELAY)

$P_D\tau_D$ = 133 fJ/GATE

Fig. 6.4-11 High speed evaluation of 5 × 5 multiplier using the on-chip P_9 to b_0 feedback path. Top photograph represents the disabling of feedback oscillations by a b_0 pulse input. The lower photograph is an expanded view of the oscillations at 109.1 MHz.

This represents a propagation delay of 208 ps/gate. When corrected for the approximately 400 ps delay introduced by the capacitance of the feedback return path, an equivalent delay per gate of 190 ps is obtained. This corresponds to a speed-power product of only 133 fJ/gate, a very acceptable level for LSI or VLSI high speed circuits. This also agrees well with what would be predicted from ring oscillator tests (see Section 6.1.) since the average logic gate size for the multiplier circuit as a whole is roughly 15 μm.

The correct performance of the 5 x 5 multiplier represents the first demonstration of a GaAs LSI circuit to ever be reported. It is very significant because it confirms the premise that GaAs SDFL circuits and the planar implanted process are capable of realizing LSI high speed circuits. The full 10 bit product is available in only 4 ns for this high speed device.

8 x 8 Multiplier

The 8 x 8 multiplier has been designed as the final 1000 gate demonstration circuit for this program. It will form the 16 bit product of two 8 bit input numbers. The multiplication is done in parallel by an array multiplier similar to the 3 x 3 or 5 x 5 multiplier described above, and the input and output words can be latched or the input can be entered directly under external control. Control of the latching, as well as the clocking, is separate for input and output. An externally activated feedback self test connection is included, similar to the one on the 3 x 3 and 5 x 5 multipliers. A block diagram is shown in Fig. 6.4-12.

An array multiplier implements the operations involved in multiplication in a straightforward way. The multiplication of two 8 bit numbers A = $a_7a_6...a_j...a$, and B = $b_7b_6..b_k..b_1b_0$ involves the sequential addition of partial sum and product terms which depend, initially, on terms that are the logical AND of individual bits of A and B, and are the forms a_jb_k. Fig. 6.4-13 depicts these operations; shown are the required bit combinations, with blocks being used to indicate adders, and arrows to indicate connection of sum and carry adder outputs to subsequent adders. Each adder block thus adds the a_jb_k term(s) shown inside and the one bit numbers represented by incoming arrows.

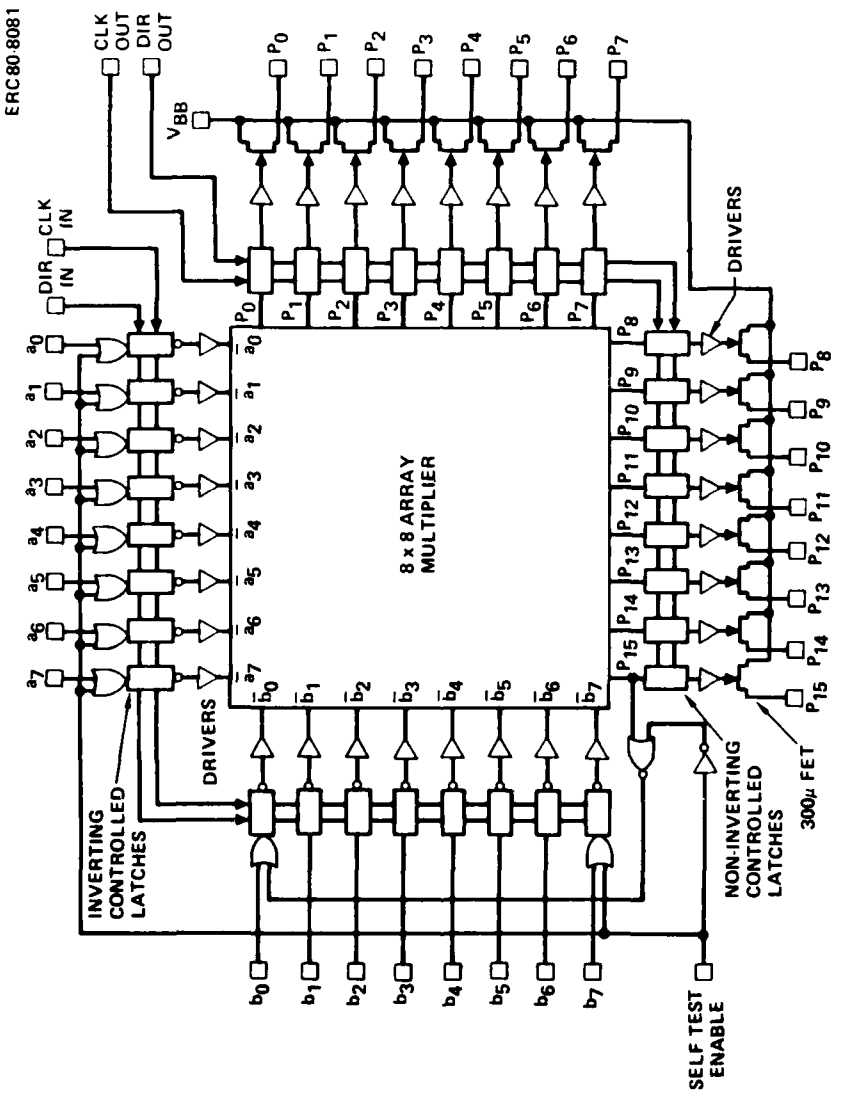


Fig. 6.4-12 Block diagram of the 8 x 8 parallel multiplier. Self test feedback path is shown on this figure.

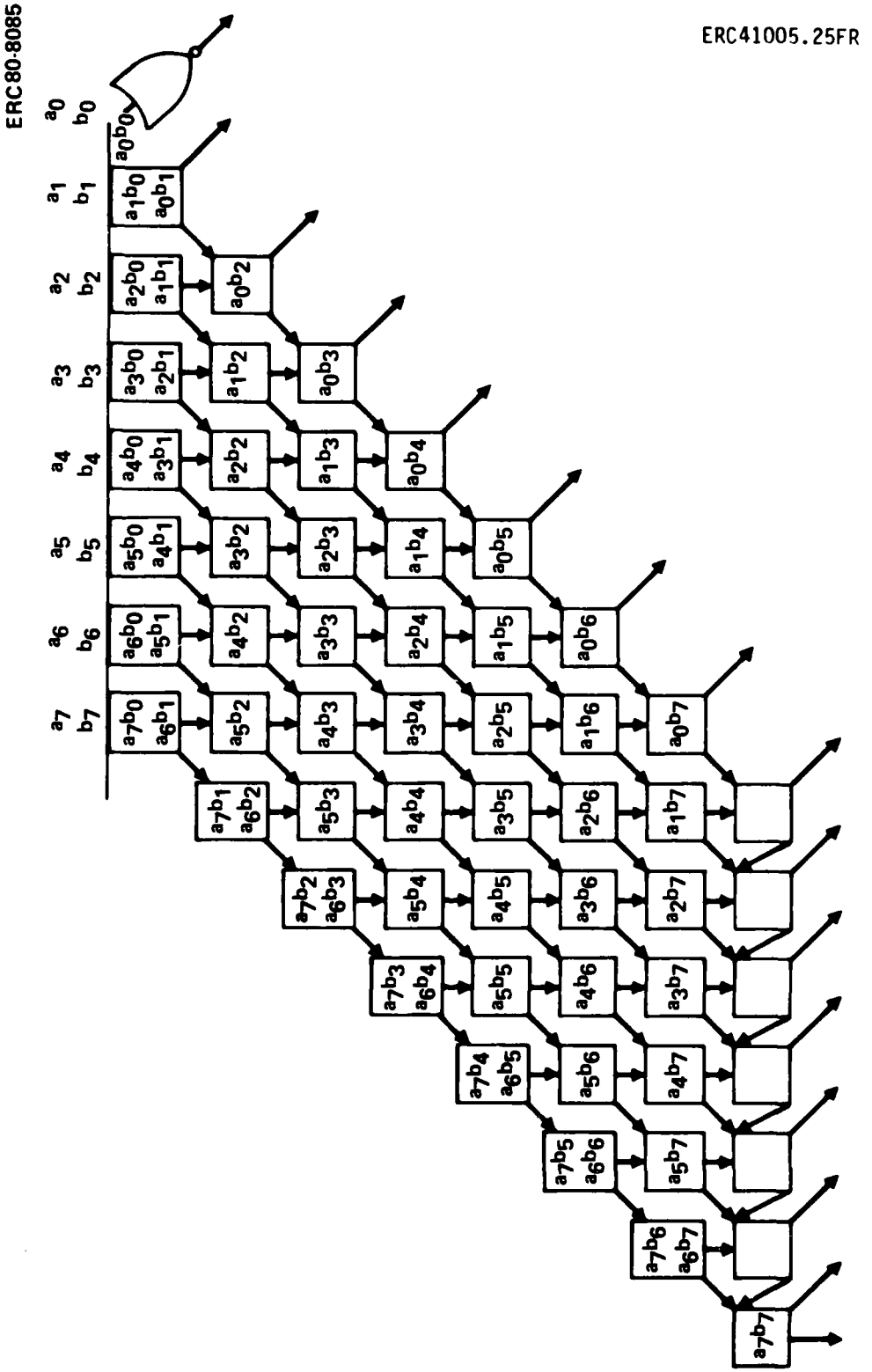


Fig. 6.4-13 Full adder array illustrating the multiplication of two 8-bit numbers.

Note that each adder block adds either two or three terms corresponding to half or full adders. In fact, the arrangement is an array of full adders except for the top row and lower right corner, which are half adders. An appropriate arrangement of adders, showing logic gates and equal interconnections is shown in Fig. 6.4-14. NOR gates are used to combine the inverses of the input bits, in accordance with the relation $\bar{a}_j + \bar{b}_k = a_j \; b_k$. This array of half and full adders and gates forms the 8 x 8 array multiplier part of the circuit.

The outputs of the array go through non-inverting controlled latches, to drivers, and then to output FETs. The non-inverting controlled latch is essentially a D flip-flop with a bypass capability to allow for asynchronous testing. When the direct control line is a one, or high, the input is routed to the output through two gates. When the direct control line is low, the input becomes latched under control of the clock, in normal D flip-flop fashion. The inverting controlled latch is just a modification of the non-inverting one.

The inputs enter via inverting controlled latches, and complementary drivers. The drivers are required to drive the considerable capacitance of the array; by implementing them in complementary form, dc power is minimized.

The self-test feedback circuit is activated by holding the enable line high. This applies "ones" to all a_j lines and to b_7. It also applies the complement of output bit P_{15} to b_0. This connection is unstable, as can be seen from the multiplication:

$$
\begin{array}{r}
A = 1\;1\;1\;1\;1\;1\;1\;1 \\
B = 1\;0\;0\;0\;0\;0\;0\;b_0 \\
\hline
b_0 b_0 b_0 b_0 b_0 b_0 b_0 b_0 \\
1\;1\;1\;1\;1\;1\;1\; \\
\hline
b_0 \bar{b}_0 \bar{b}_0 \bar{b}_0 \bar{b}_0 \bar{b}_0 \bar{b}_0 \bar{b}_0 \bar{b}_0 b_0 b_0 b_0 b_0 b_0 b_0 b_0 b_0
\end{array}
$$

Changing bit b_0 (from 1 to 0 or 0 to 1) involves the longest delay path through the multiplier array, as can be seen from Fig. 6.4-13 and 6.4-14. Since the delay to a sum output for an SDFL NOR implemented adder is $3\tau_d$ and for a

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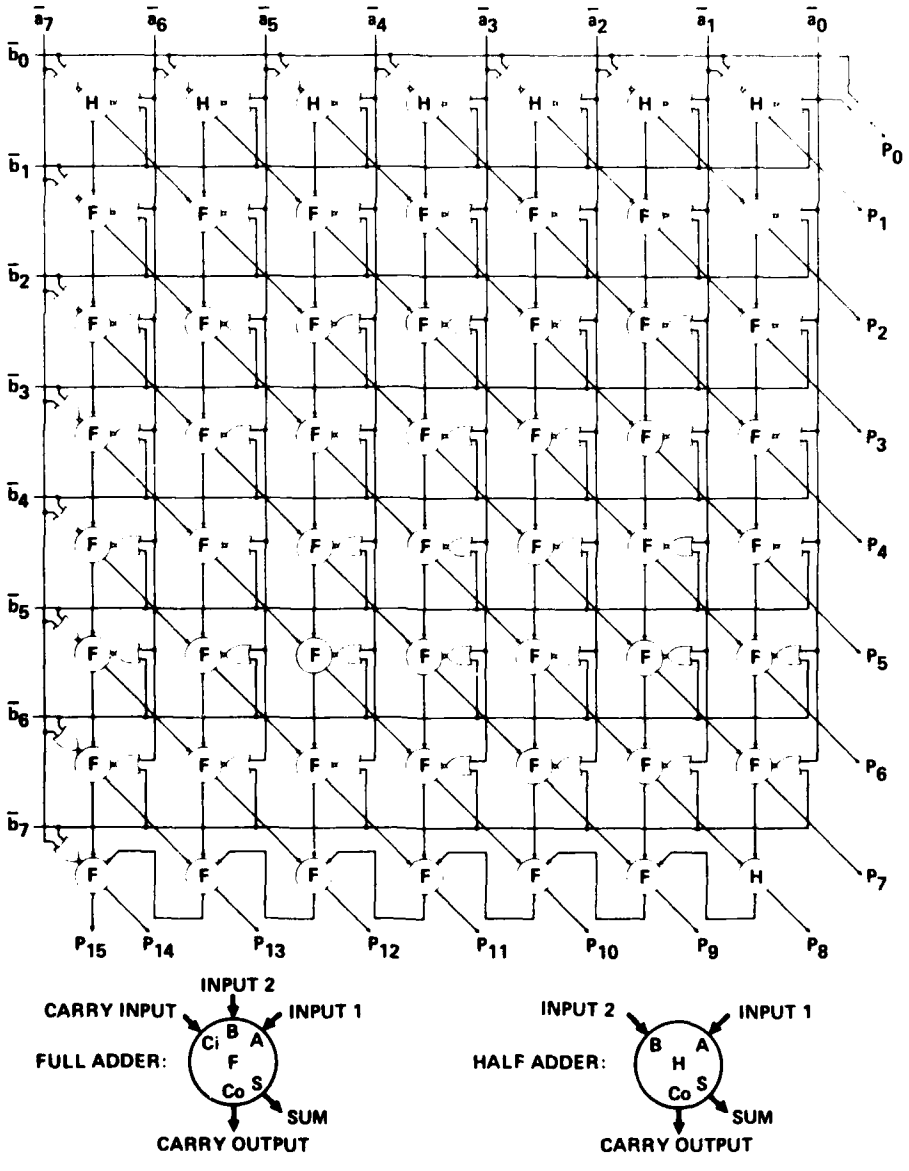

Fig. 6.4-14 Circuit diagram of 8 × 8 parallel multiplier array.

carry is $2\tau_d$, the delay to the most significant product bit (P_{15}) is 6 sums and 8 carries for a total of $34\tau_d$. Adding the control and latch gates, the self test mode causes the multiplier to self oscillate with half-period of approximately $40\tau_d$.

Operation is therefore possible in three modes; with inputs and outputs unlatched (straight parallel multiplier); with inputs and/or outputs latched and independently clocked; and in an oscillatory self test mode. The 8 x 8 multiplier clearly represents an LSI chip. The array multiplier has 688 gates and the latches add 256 for 944. Including driver and control gates, the total is 1008.

The layout is designed as an array of cells. The full and half adders are organized as cells, as are the inverting controlled latch (ICL) and the non-inverting controlled latch (NICL). The layout is then as shown in Fig. 6.4-15. This overall chip organization allows the complete circuit to be constructed by straightforward application of the Calma GDS-II software. Minimizing the number of individual circuit cells reduces the probability of design error by allowing for exhaustive inspection of only a limited number of cells. This approach is essential to the efficient design of error-free LSI chips.

The complete 8 × 8 parallel multiplier circuit was placed in a 2.7 mm x 2.25 mm chip area including bonding pads and was located on mask set AR5. A photograph of a multiplier chip is shown in Fig. 6.4-16. As a result of the LSI design approach mentioned above, no mask design errors have been found on the 8 × 8 multiplier.

The multiplier circuit has been evaluated for logic functionality of all sections of the circuit and for high speed performance. While only a few wafers had been evaluated to the reporting date, significant numbers of partially functional chips have been identified. This means that all but one or two of the 16 product bits was providing the correct output codes. One of the chips evaluated was so close to full operation that its performance could be accounted for with only 2 out of the 1008 gates not being effective. Because of the small number of chips on each wafer (32) and the small number of wafers

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	a_6	a_5	a_4	a_3	a_2	a_1	a_0	
b_0	ICL	ICL	ICL	ICL	ICL	ICL	ICL	ICL	
b_1	ICL	HA	HA	HA	HA	HA	HA	HA	NICL
b_2	ICL	FA	FA	FA	FA	FA	FA	FA	NICL
b_3	ICL	FA	FA	FA	FA	FA	FA	FA	NICL
b_4	ICL	FA	FA	FA	FA	FA	FA	FA	NICL
b_5	ICL	FA	FA	FA	FA	FA	FA	FA	NICL
b_6	ICL	FA	FA	FA	FA	FA	FA	FA	NICL
b_7	ICL	FA	FA	FA	FA	FA	FA	FA	NICL
a_7	ICL	FA	FA	FA	FA	FA	FA	HA	NICL
		NICL	NICL	NICL	NICL	NICL	NICL	NICL	NICL

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Fig. 6.4-15 Layout of 8 × 8 multiplier. This multiplier is designed of an array of cells consisting of inverting control latches, non-inverting control latches, half adders, and full adders.

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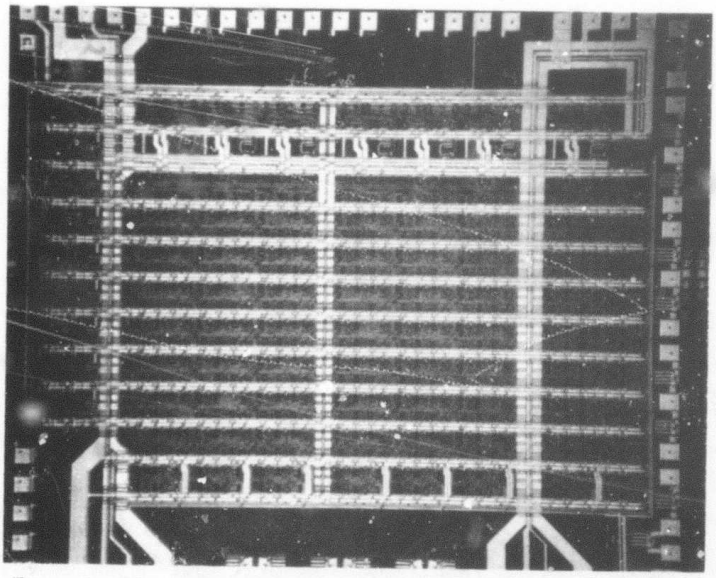

Fig. 6.4-16 Photomicrograph of an 8 × 8 multiplier chip. The chip including bonding pads covers a 2.7 mm × 2.25 mm area.

evaluated to date, it is considered very likely that a fully functional 8 × 8 chip will be found in the future.*

Figure 6.4-17 shows the performance of the 8 × 8 multiplier in an unlatched (asynchronous) ripple test where the product 255 × 128 is being performed with a pulse applied to the b_0 input. The output product bits P_0 to P_{15} are shown to have the proper relationship to the b_0 input in this figure. Power dissipation ranged generally from 1 to 2.2 W total for the relatively high pinchoff voltage wafers (V_p = -1.2 to - 1.6 V) evaluated to date.

Figures 6.4-18 and 6.4-19 depict the performance of the multiplier circuits operating synchronously with input and output latches respectively. A b_0 data input was derived from the clock waveform by a TTL frequency divider so that the data edge transitions were no longer coincident with all of the falling clock edges. This makes the DFF latch functionality evident by comparing the product output transitions with the clock and data inputs. Note that all input and output latches in Fig. 6.4-19 are working except the P_3 output which is switching prematurely. This is a consequence of one defective gate in the P_3 output latch.*

High speed performance evaluation was also carried out using the on-chip feedback path (as was done on the 3 × 3 and 5 × 5 multipliers). The latches were operated with the direct control line high (logical "1") so that the multiplier would operate asynchronously. Figure 6.4-20 illustrates the oscillatory output waveform resulting from this test. The oscillation frequency observed in this case was 83.1 MHz which corresponds to a propagation delay per gate of 150 ps ($f = 1/80\ \tau_d$). This results in a full 16 bit product being performed in only 5.2 ns, a significant achievement. It is also important to note that speed was not compromised on the multiplier circuits by scaling up to the 1000 gate LSI level of complexity. In fact, the 8 × 8 multiplier average

*While this report was in press, full operation of the 8 × 8 bit parallel multiplier, including both the multiplier array and all the latches, was determined.

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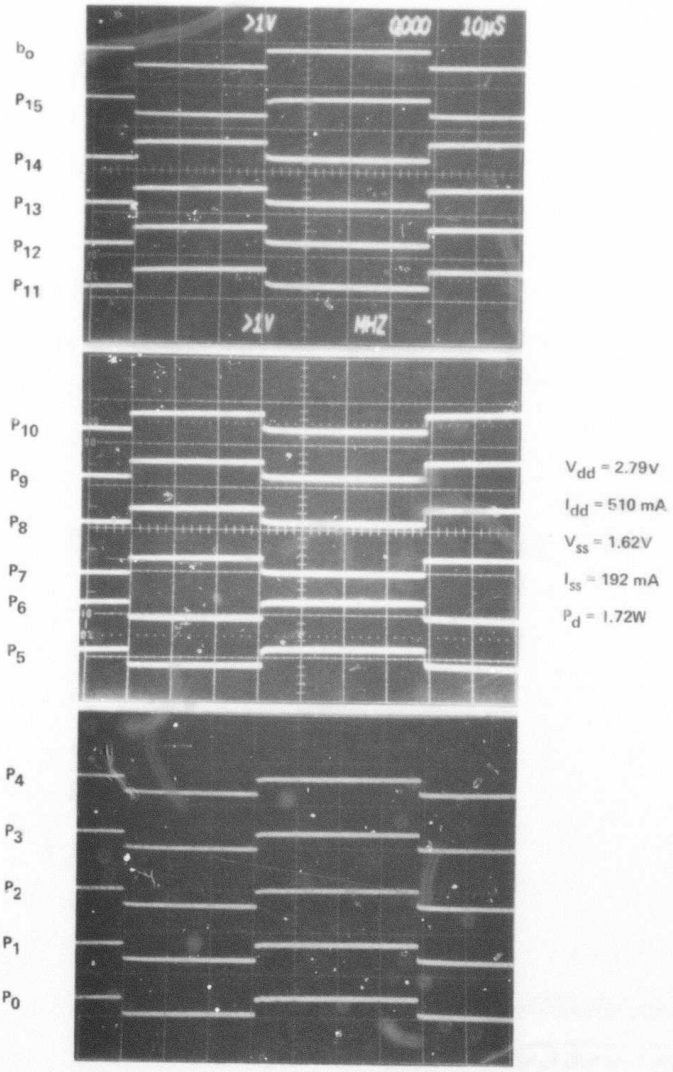

Fig. 6.4-17 Ripple (asynchronous) test of 8 × 8 multiplier with pulse input at b_0.

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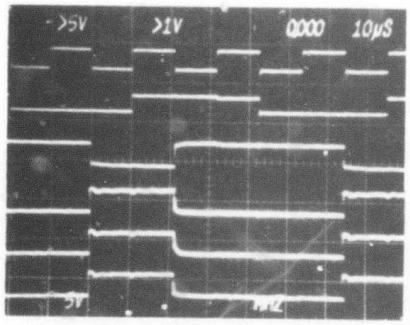


CLOCK

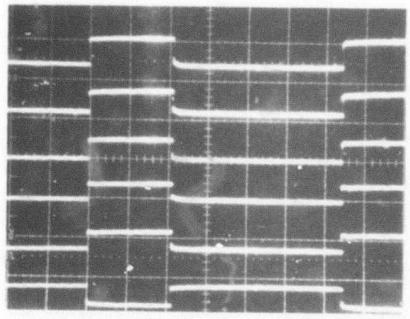
DATA IN (b_0)

P_{15}

P_{14}

P_{13}

P_{12}



P_{11}

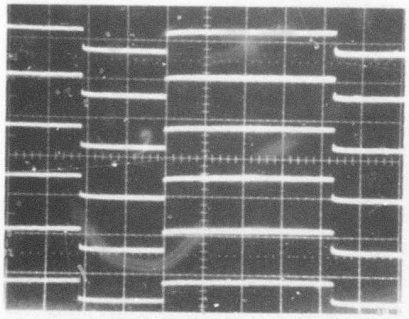
P_{10}

P_9

P_8

P_7

P_6



P_5

P_4

P_3

P_2

P_1

P_0

255 x 128

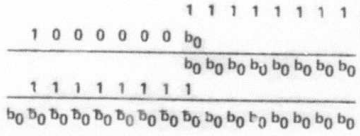


Fig. 6.4-18 Performance of 8 × 8 multiplier when data input is controlled by the input latches. Note that the output transitions are now synchronous with the falling clock edge.

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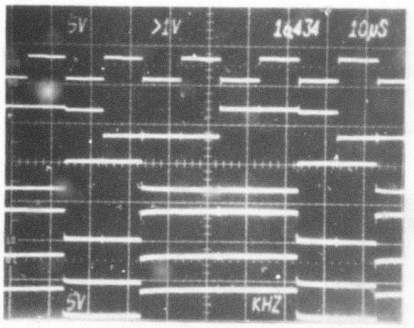


CLOCK

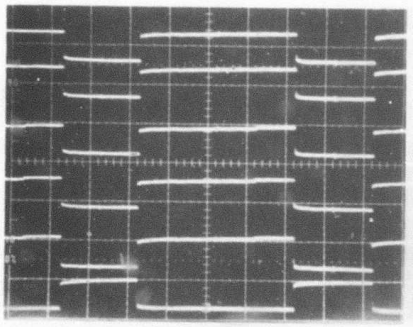
DATA IN (b_0)

P_{15}

P_{14}

P_{13}

P_{12}



P_{11}

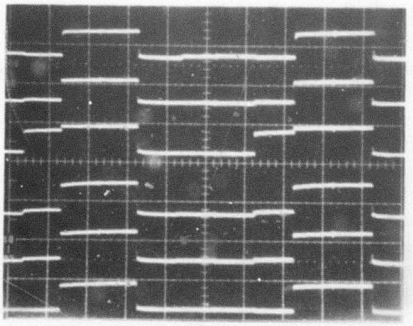
P_{10}

P_9

P_8

P_7

P_6



P_5

P_4

P_3

P_2

P_1

P_0

255 x 128

Fig. 6.4-19 Performance of 9 x 8 multiplier when data output is controlled by the output latches. Note that the output transitions are now synchronous with the falling clock edge.

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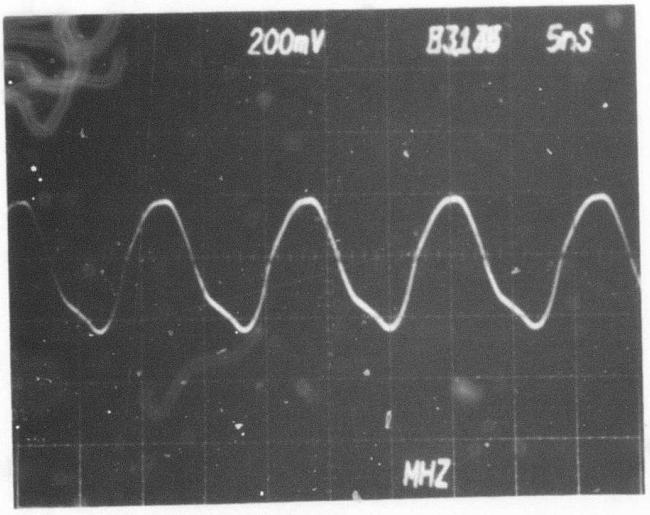

V_{dd} = 2.72V f = 83.1 MHz τ_d = 150 ps

V_{ss} = -2.03V P_d = 2.08W $P_d\tau_d$ = 310 fJ

Fig. 6.4-20 Performance of 8 × 8 multiplier when evaluated for high speed operation. The on-chip feedback path was enabled and the latches disabled to perform this measurement.

gate delays were less than those observed on the 75 gate 3 × 3 MSI multiplier, probably a consequence of improved design. Total power dissipation of the 8 × 8 multiplier chip was 2.08 W or ~ 2 mW/gate.

6.5 Circuit Packaging

The three stage binary ripple divider circuit (divide by 8) was chosen for packaging studies and for delivery of MSI packaged circuit samples. This circuit is implementred with T-connected D Flip-Flops as described in Section 6.3. Two versions of this circuit were packaged and delivered. For the first set of deliverables, chips from mask set AR3 were identified at wafer probe, then diced and bonded. Low bonding yields were obtained on the AR3 chips due to the very tight pad spacing (10 μm) and small pad sizes (65 μm). Thus, the second set of deliverables was obtained from a redesigned divide-by-8 circuit. This chip had increased spacing (25 μm) and pad sizes (75 μm × 75 μm) which made bonding much more easily accomplished.

All divider chips were bonded into 16 pin flat-packs with 0.030" center-to-center spacing between leads (Mini System #3H16M-1). The depth of this package allows diced circuits to be placed directly into the package with no additional lapping. The small dimensions of this package help to minimizing lead inductance and ringing effects.

The packaged divider circuits were evaluated in the microstrip test fixture shown in Fig. 6.5-1. This fixture provided for convenient mounting and demounting of the flat-packs, using a pressure contact of the leads to an alumina circuit board. All high speed inputs and outputs used 50 Ω microstrip transmission lines and SMA connectors. All high-speed inputs and outputs were terminated with 50 Ω chip resistors as close to the package as possible. The clock sine wave input was offset by dc bias using a broadband bias tee.

The performance of packaged dividers delivered in the first set of samples is summarized in Table 6.5-1. Here, a maximum clock frequency of almost 1.8 GHz was observed. This is considerably higher than the 1.5 GHz maximum observed on these devices when characterized on the wafer using a conventional probe card. This improvement in performance is attributable to the improved

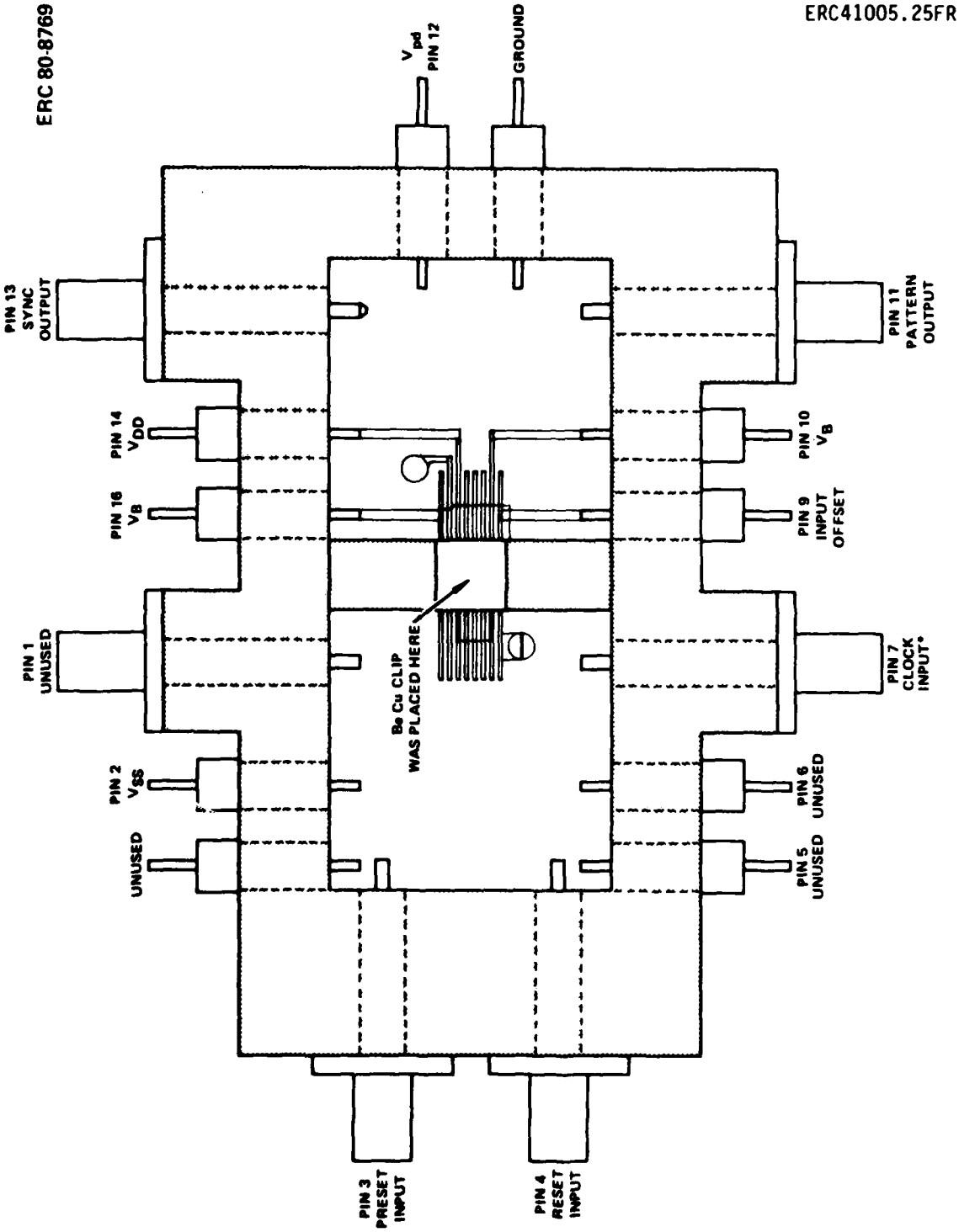

Fig. 6.5-1 Test fixture for evaluation of packaged binary ripple dividers.

grounding, impedance matching and shorter lengths of unterminated line which are possible with the flat pack implementation. Maximum operating frequencies achievable at wafer probe were generally associated with resonance phenomena and ground noise. The bias conditions and maximum clock frequency observed on the five deliverable chips in Table 6.5-1 varied from device to device because the samples were taken from three different AR3 wafers.

The second set of packaged divider samples were obtained from RD-2 wafers (from an IR&D program), and the performance and operating conditions are summarized in Table 6.5-2. The operating characteristics of the 5 packaged devices here were much more uniform than those in Table 6.5-1 because they were all taken from the same wafer. Maximum clock frequencies as high as 1.5 GHz were achieved with power dissipations of the order of 100 mW. Additional packaged device samples were also provided for radiation hardness and temperature range evaluations as discussed in Section 6.6.

6.6 Environmental Testing

Temperature Dependence of IC Operation

Since operation of GaAs IC above room temperature will ultimately be required, measurements of isolation, FET I-V characteristics, SDFL NOR gate transfer characteristics and ring oscillator dynamic characteristics have been made over the range of 25° to 200°C. Elevated heat sink temperatures were achieved on a high speed probe station using a small hot plate fabricated on an alumina substrate supported by standoff insulators.

In circuits with potentially high packing density, such as SDFL, adequate isolation between adjacent regions, interconnections and devices is essential to prevent the occurrence of logic errors and circuit malfunctions. To evaluate the degree to which this isolation affects or may potentially affect areas separated by very small gaps, the T1 test structure shown in Fig. 5.2-1 was chosen. This test structure was repeated throughout the wafer. Here, two ohmic contacts on n^+ implanted GaAs are separated by a 3 μm gap of unimplanted, semi-insulating GaAs. This gap is representative of the minimum line separations which might be encountered in a densely packed circuit. The width of these regions is 50 μm.

Table 6.5-1

Summary of Packaged Divider Performance from Wafer AR3

Package Number	V_{DD}(V)	V_{ss}(V)	I_{DD}(mA)	I_{ss}(mA)	V_{offset}(V)	V_B(V)	f_{max} (Ghz)	P_d(mW)	Notes
A	2.415	-1.79	23.5	-6.8	12.31	1.32	1.78	68.9	Low +8 output amplitude
C	2.80	-1.46	21.9	-5.9	15.24	2.72	1.40	69.8	
D	2.69	-1.99	19.0	-5.5	12.82	2.13	1.34	62.0	
E	2.62	-1.20	28.9	-6.0	13.47	2.86	1.71	83.0	
G	4.96*	-1.34	30.8	-5.9	13.93	4.96*	1.24	153.5	Low +8 output amplitdue
							$V_B = V_{dd}$		

*V_{dd} is tied to V_B, possibly due to bonding problems.

Table 6.5-2

Summary of Packaged Divider Performance from RD2

Package	V_{DD}(V)	V_{ss}(V)	I_{DD}(mA)	I_{ss}(mA)	V_{PD}(V)	V_B(V)	f_{max}(GHz)	P_d(mW)
1	3.0	-1.6	28.4	-6.4	-2.0 +3.0	1.37	95.4	
5	3.0	-1.6	29.1	-5.9	-2.1 +3.0	1.4	96.7	
6	3.0	-1.6	31.9	-6.7	-2.05+3.0	1.5	106.7	
8	3.0	-1.6	28.5	-6.2	-2.03+3.0	1.41	95.4	
9	3.0	-1.6	29.7	-6.2	-2.06+3.0	1.4	99	

Three wafers were selected for evaluation of isolation. They were fabricated on substrate material from two ingots, from which wafers have been supplied as a contract deliverable item (ingots #3396 and #3475). Currents between the contacts were measured up to approximately 5 V of bias from room temperature to 200°C. The samples were biased through probes, and the currents were measured with a Tektronix 577 curve tracer which is capable of resolving 1nA currents.

The results of isolation measurements on wafer AR1-22 (substrate #3475) are presented in Fig. 6.6-1. Current vs voltage characteristics at four temperatures are plotted on log-log scales. Since normal worst case circuit potential differences would be approximately 3V, substrate sheet resistivity was calculated assuming an ohmic I-V characteristic at that voltage. For this wafer, resistivities of 2.5×10^8 Ω/□ at 25°C and 1×10^6 Ω/□ at 200°C were calculated. Maximum leakage currents at the 3V level were 60 μA, still two orders of magnitude below normal circuit current in a comparable 50 μm FET. A summary of measured sheet resistivities for this wafer and two other wafers is shown in Table 6.6-1. All of these measurements were made on wafers which had completed all of the fabrication processes. The main mechanism responsible for current flow appears to be space charge limited current and the gradual degradation of resistivity probably relates to the thermal ionization of deep centers in the Cr-doped GaAs substrate.

Table 6.6-1

Substrate Sheet Resistivities at 3V Bias.
Measurements Made on Test Cell T1, 3 μm Gap × 50 μm Wide Isolation Test

Sample Number	ρ_S (Ω/□)	Temperature (°C)
AR1-3	1.5×10^{10}	23
AR1-3	2.5×10^7	133
AR1-9	8.3×10^9	23
AR1-9	3.3×10^7	105
AR1-22	2.5×10^8	25
AR1-22	1.0×10^6	200

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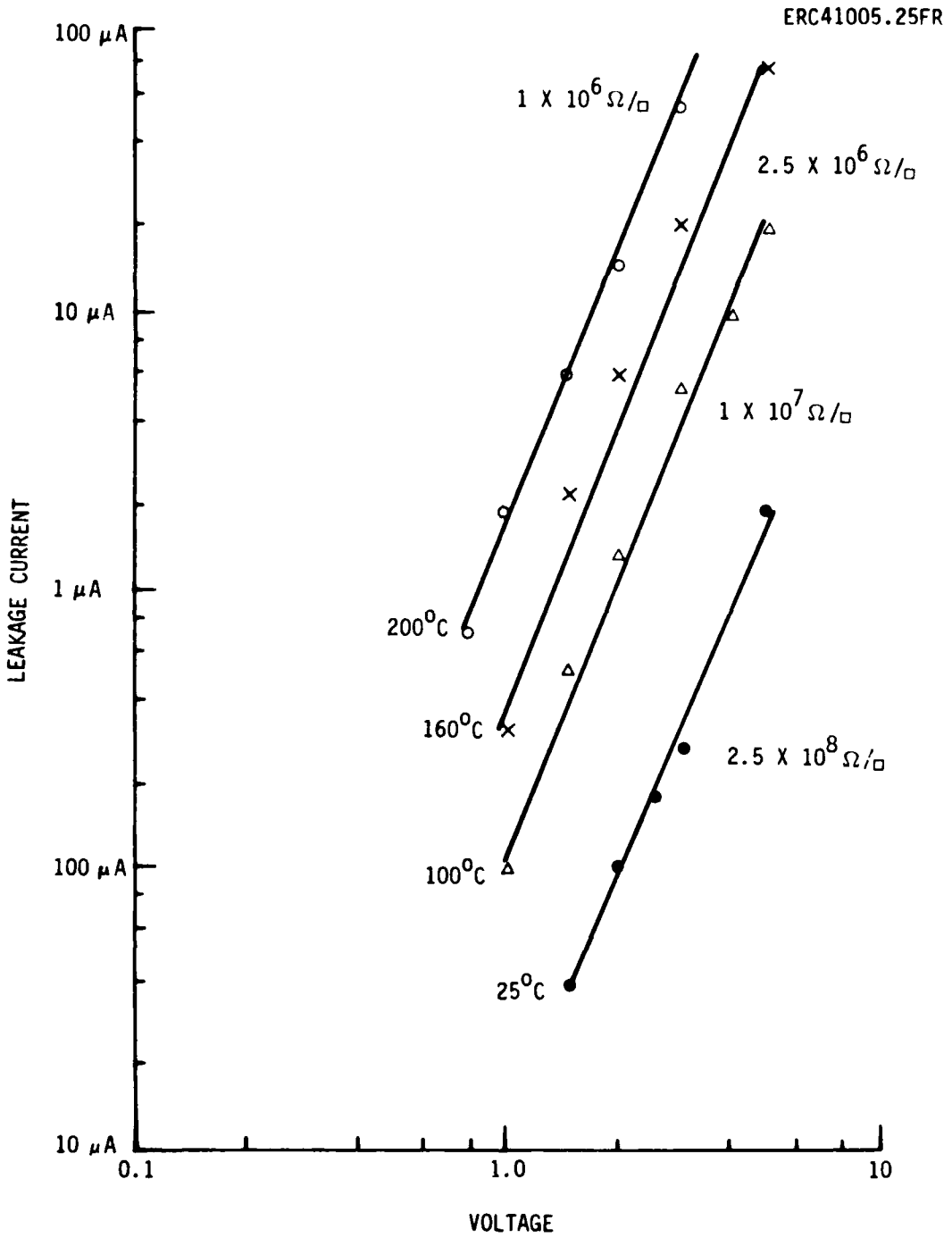

Fig. 6.6-1 Isolation measurement on test cell T1.

Drain current as a function of V_{ds} and V_{gs} was also measured over the same temperature range for a 1 μm × 50 μm FET located in test cell T2 (see Fig. 5.2-1). The I_{ds} vs V_{gs} characteristic was measured with a constant V_{ds} = 2.5 V. The results of this measurement are presented in Fig. 6.6-2. The approximately 17% reduction in drain current which was observed at the highest temperature is expected from the decrease in mobility and electron drift velocity with increasing temperature. There was no change in either V_{dss} or the pinch-off voltage of this device over the above range.

The transfer characteristic of an SDFL NOR gate should be even more sensitive to temperature since three FETs and two diodes are interconnected in the simplest case. Large shifts in the characteristics of any of the above devices would be detectable in measurements of the input vs output behavior of the gate. Therefore, measurements were made over the 23° to 200°C temperature range on a 10 μm NOR gate located in test cell T2. This consists of a 2 input gated with level shift diode utilizing a 10 μm inverter, 2 μm pull-down and 7 μm pull-up FETs. This gate is also shown in Fig. 5.2-1.

Fig. 6.6-3 presents the gate output voltage, and the currents I_{dd} and I_{ss} as functions of input voltage at three operating temperatures. The supply voltages, V_{dd} and V_{ss}, were held constant. No change in the output voltage for a low output was observed. At 200°C, a reduction of high output voltage by 0.2 V was observed. The threshold voltage of the gate, defined by the intersection of the transfer characteristic with the $V_{IN} = V_{OUT}$ line, decreased slightly from 1.7 V to 1.4 V at the maximum temperature. Slight increases in I_{dd} and I_{ss} were evident as temperature was increased.

Finally, ring oscillators consisting of 9 stages of 10 μm SDFL NOR gates were measured up to 200°C to determine the influence of temperature on the dynamic performance of a more complex circuit. Results of this measurement at three temperatures are summarized in Fig. 6.6-4. Spectrum analyzer scans from 0 to 1 GHz are shown at each temperature. Bias voltages were chosen for operation at moderate frequencies rather than maximum speed or lowest $P_d\tau_D$ product. Note that the distribution of power between the three spectral components falling in this frequency range shifts slightly as temperature varies. This implies that

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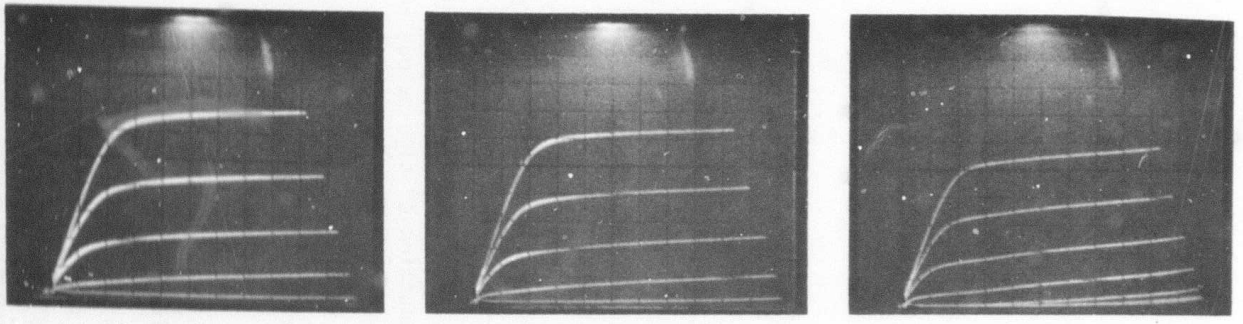

25° 100°C 200°C

Fig. 6.6-2 Elevated temperature evaluation of 50 μm FET.
Vertical scale: I_{DS} = 1 mA/div
Horizontal scale: V_{DS} = 0.5 V/div
Step generator: V_{GS} = 0.5 V/step.

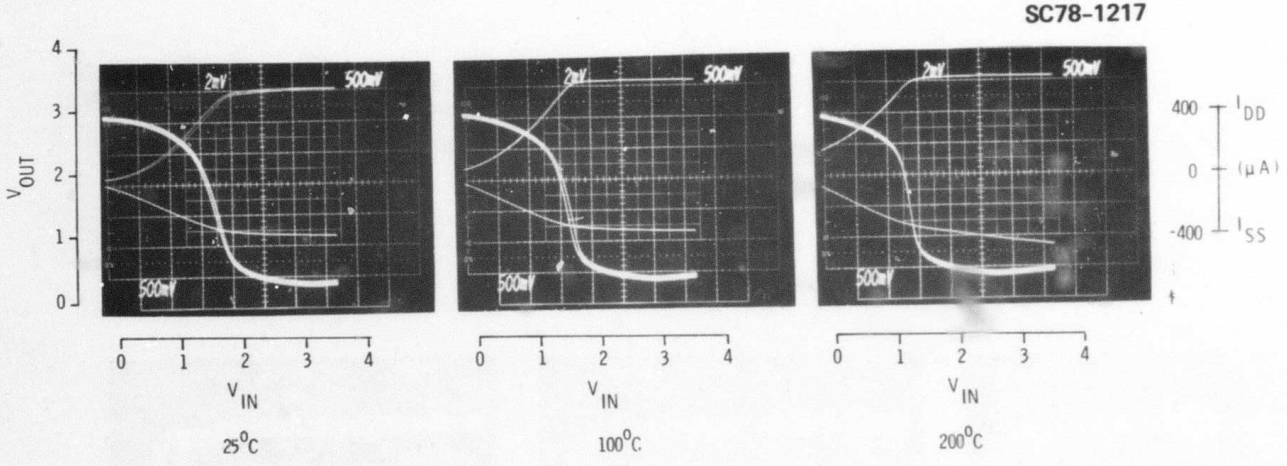

Fig. 6.6-3 Elevated temperature evaluation of 10 μm SDFL NOR gate.

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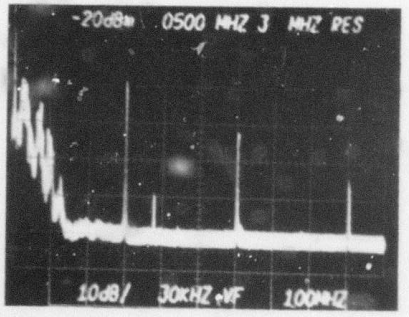


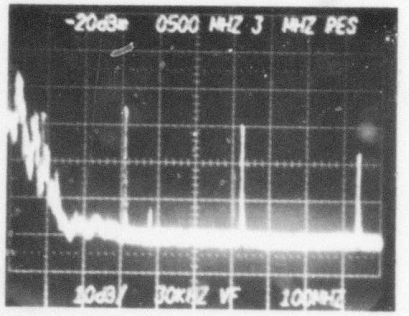
$25^{o}C$

f = 297.5 MHz

T_D = 187 pS

P = 0.6 mW/GATE

P_{TD} = 0.11pJ



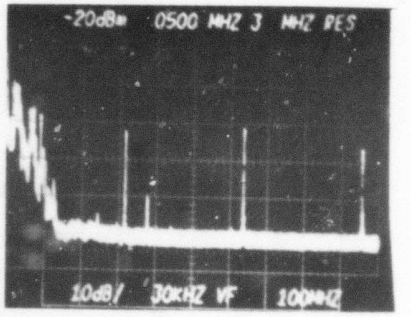
$100^{o}C$

f = 318 MHz

T_D = 175 pS

P = 0.86 mW/GATE

P_{TD} = 0.15pJ/GATE



$200^{o}C$

f = 310 MHz

T_D = 179 pS

P = 1.49 mW/GATE

P_{TD} = 0.27pJ/GATE

Fig. 6.6-4 Elevated temperature evaluation of SDFL ring oscillators. (9 stage, 10 μm NOR gates).

the time domain waveform is changing shape. However, propagation delay or operating fundamental frequency remains relatively constant. The increased speed at elevated temperature is due to increasing I_{dd} and I_{ss} which results in more rapid charging of output capacitances.

The results of these four measurements, which have been repeated on several wafers with the same results, strongly indicate that loss of adequate isolation at elevated heat sink temperatures does not occur on qualified substrate material. Device performance will not be significantly degraded by elevated temperature. Although such satisfactory results had been expected, based on the physics of semi-insulating GaAs, it is very encouraging to verify them experimentally.[40]

Performance of packaged 3 stage ripple dividers (divide by 8) circuits, fabricated on the Rockwell IR&D program, have been evaluated for operation over the -50°C to +100°C temperature range as part of the IR&D packaged device evaluation effort. The results of the evaluation in the -50°C to +50°C temperature range show successful operation. No changes in biasing conditions were necessary over this temperature range. Speed-power products were slightly improved at low temperatures as a consequence of the high speeds and lower power levels observed. Above 50°C, slight bias voltage changes were sufficient to maintain correct operation up to 100°C. As part of the IR&D effort the above divider circuits were also tested at 77°K (LN_2) temperature. Here, normal operation of the circuit was also maintained indicating well behaved material, device and circuit properties, even at extremely low operating temperatures.

Radiation Hardness Assessment

The successful application of GaAs high speed digital circuits in a space environment is dependent on a sufficiently large total dose radiation hardness. While GaAs MESFET ICs are expected to be superior to silicon MOS devices (small device area, no oxide, semi-insulating substrate), this expectation must be verified by experiments on GaAs planar ICs. A summary of data from total dose radiation hardness evaluation reported for a variety of GaAs devices is presented in Table 6.6-2. It can be seen from this table tha GaAs total dose

hardness is very promising for ICs, CCDs, JFETs and discrete MESFETs. A total dose of 10^6 rads is considered to be worst case exposure for typical satellite applications. Degradation mechanisms reported in the literature[41-43] for GaAs devices are threshold voltage shift and mobility degradation. However, for FET channels doped at 10^{17} cm^{-3} these effects have been insignificant even at 10^8 rads doses.

Table 6.6-2

Radiation Hardness (Total Dose)

Device	Total Dose (rad) (X-ray or Gamma)	Results
GaAs IC dividers (÷8) (Rockwell)	5×10^7	No change of maximum clock rate
GaAs CCD (Rockwell)	2×10^6	No observable gate threshold shifts
GaAs Enhancement-Mode JFET Ring Oscillator (41, 42)	10^7	Negligible threshold shift or current degradation
GaAs MESFET-Discrete (43)	8×10^7	Negligible threshold shift or current degradation

Preliminary experiments on Rockwell GaAs planar integrated circuits (first row on Table 6.6-2) are very promising. Three packaged ÷8 circuits were irradiated at RADC with total gamma doses of 10^6, 10^7 and 5×10^7 rad, respectively. The results of this evaluation are shown in Table 6.6-3. The circuits were found fully operational after irradiation. The maximum clock rates for all circuits had not changed. The only noticeable changes were small variations in the optimum bias voltages and corresponding currents. However, these small changes may be attributed to uncertainties in the test fixture. These excellent results tend to confirm the expectations for GaAs ICs. However, a more thorough investigation is still needed.

Table 6.6-3

Planar SDFL Divided by 8
Radiation Hardness Evaluation

Device	Total Dose (Rad)	Before			After		
		V_{dd} (V)	I_{dd} (mA)	F_{max} (GHz)	V_{dd} (V)	I_{dd} (mA)	F_{max} (GHz)
RD2 #10	1×10^6	3.8	18.8	1.07	4.0	15.1	1.08
RD2 #12	1×10^7	2.2	14.4	1.14	2.3	13.4	1.14
RD2 #51A	5×10^7	2.1	11.6	1.22	2.1	10.6	1.22

7.0 PUBLICATIONS

This section contains a list of publications based totally or in part on work performed under this contract.

1. R.C. Eden, "The Prospects for Ultra High Speed VLSI GaAs Digital Logic," Device Research Conf., June 1978, Santa Barbara, CA.

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